

FIG. 1

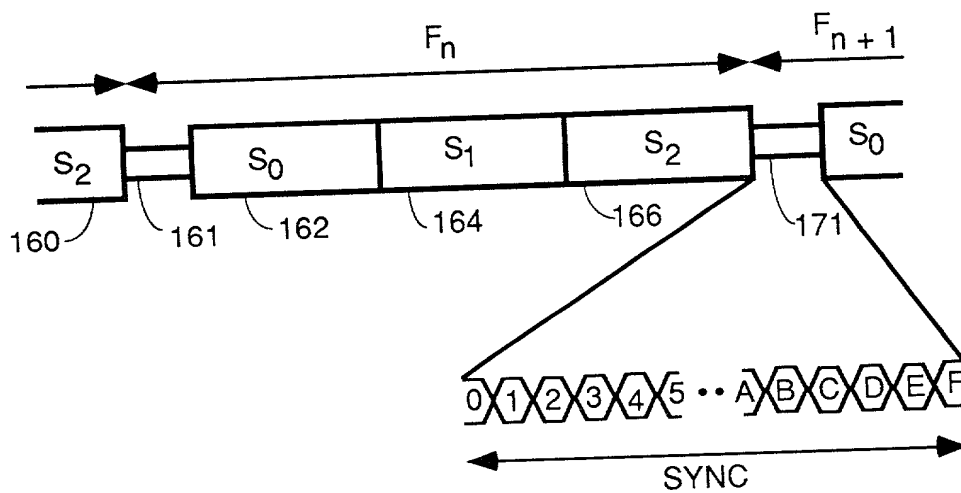


FIG. 2A

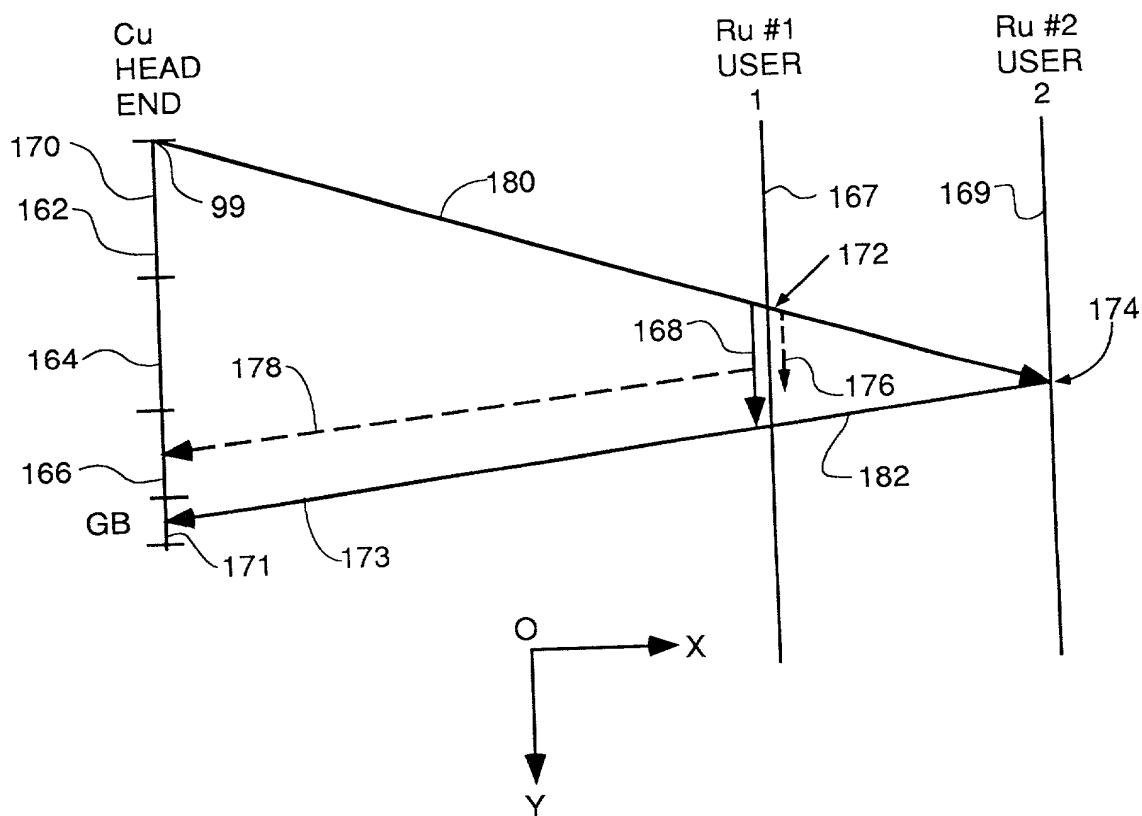


FIG. 2B

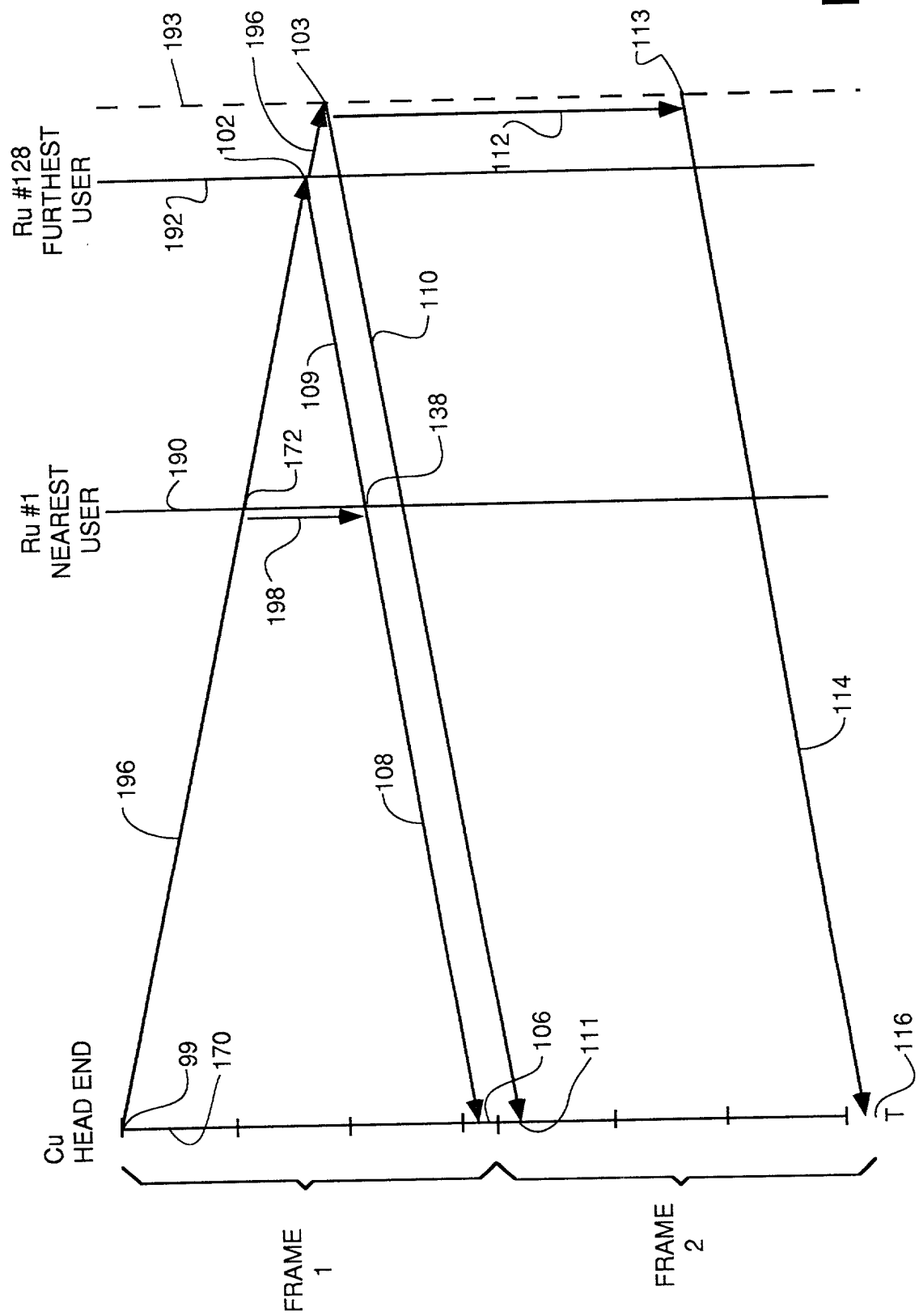


FIG. 3

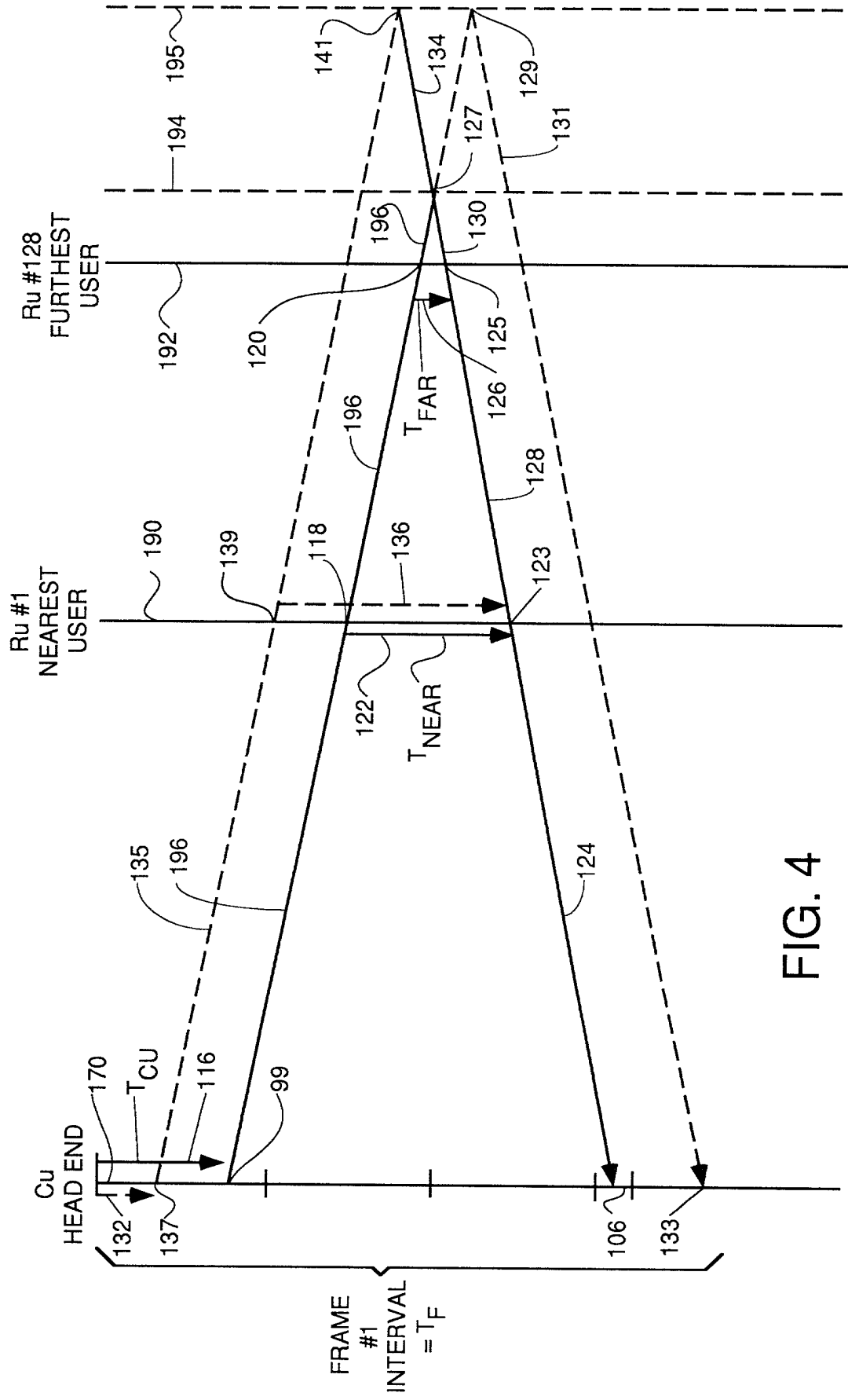
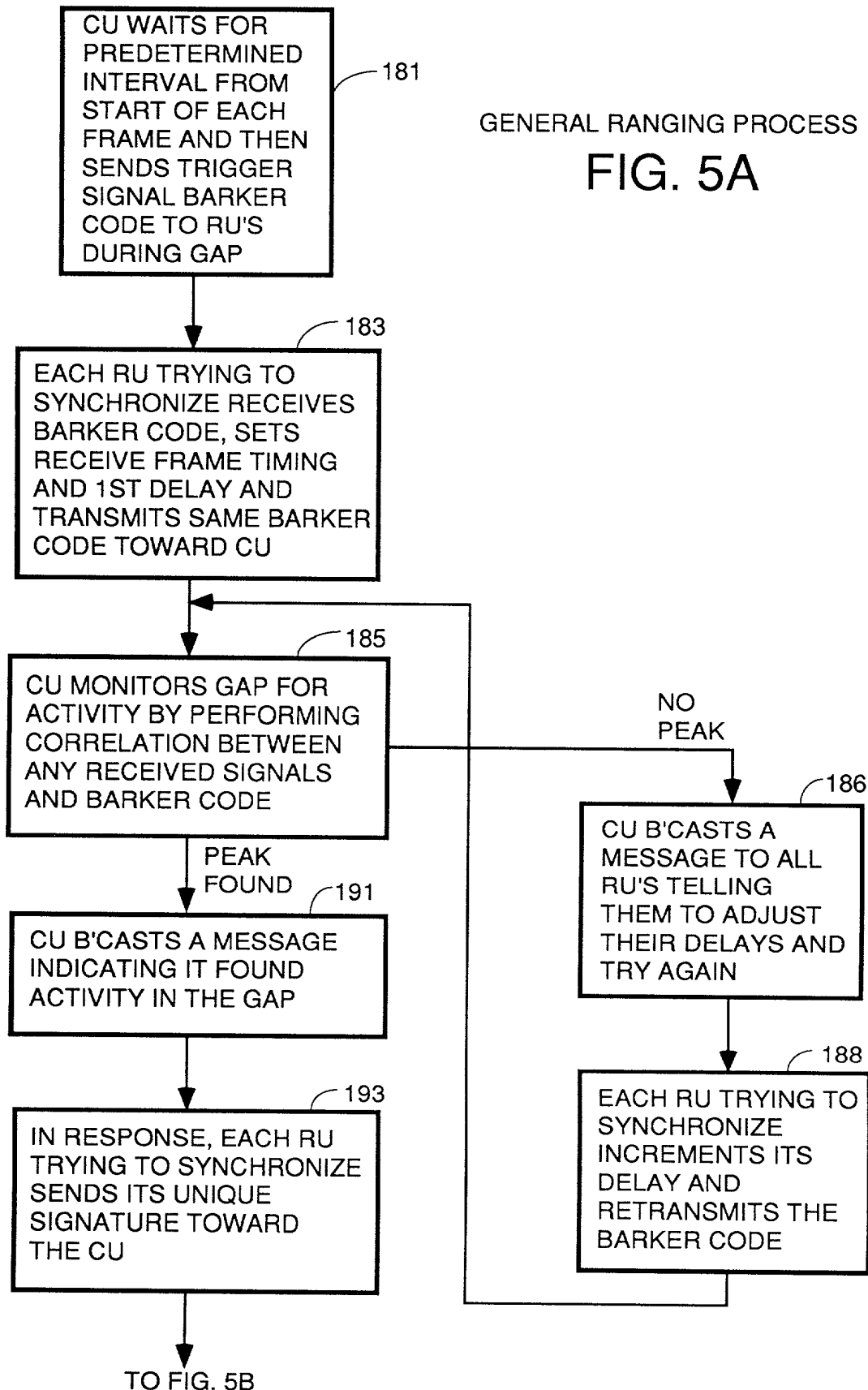


FIG. 4

# GENERAL RANGING PROCESS

## FIG. 5A



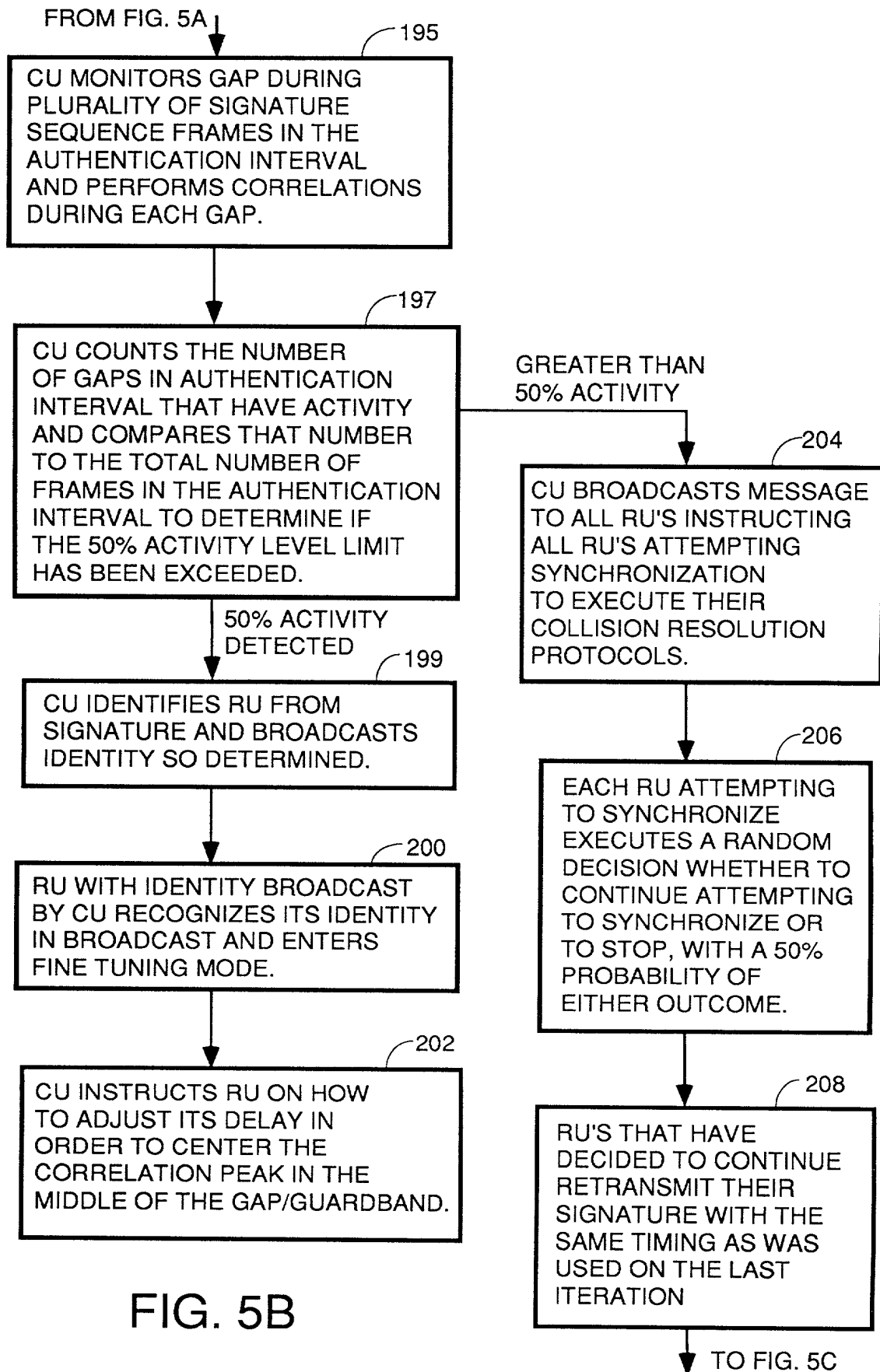


FIG. 5B

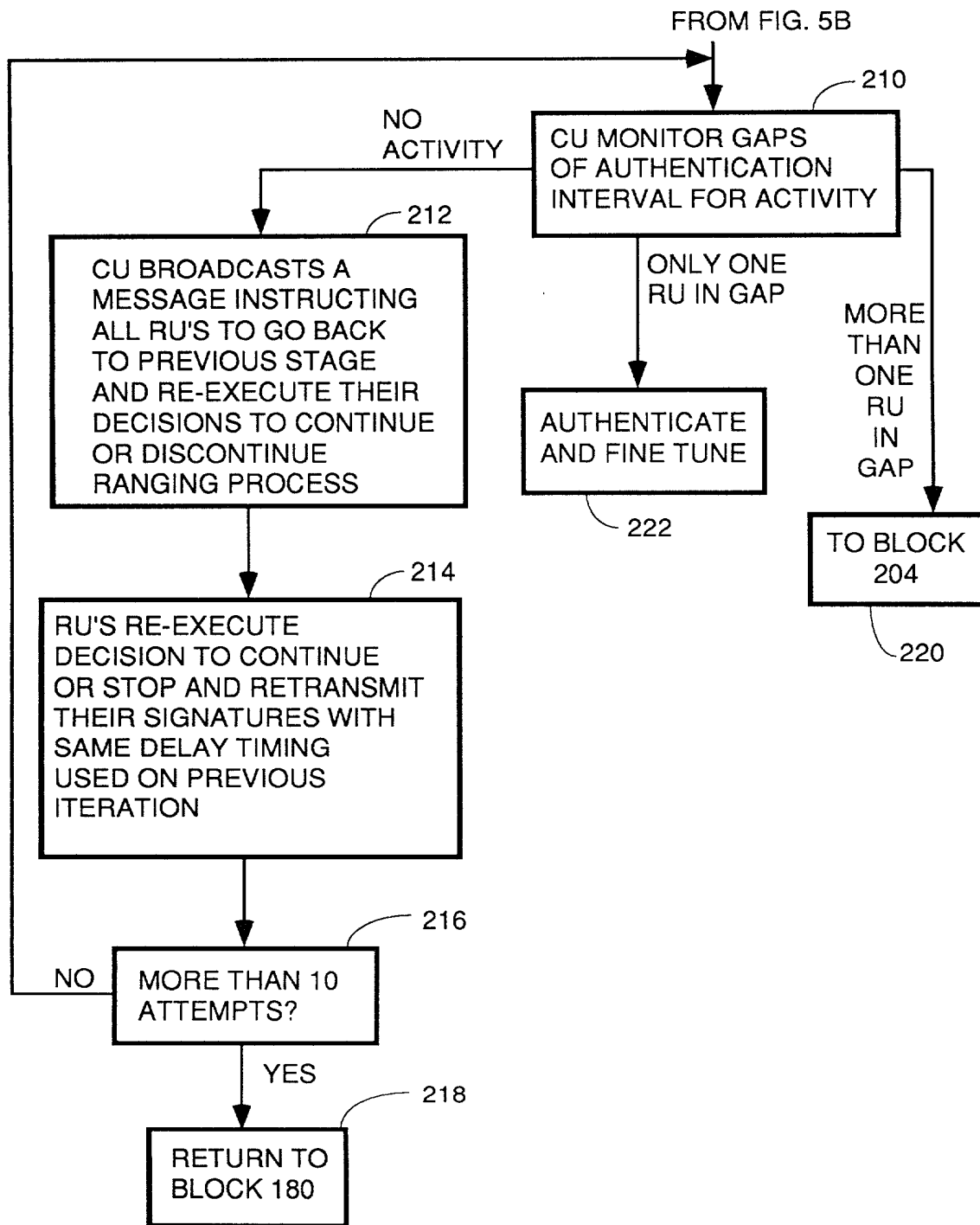
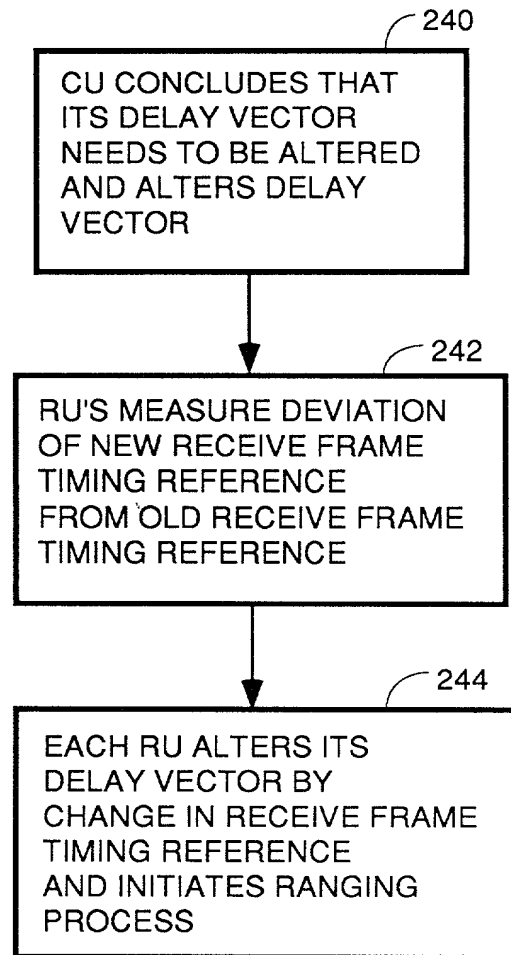
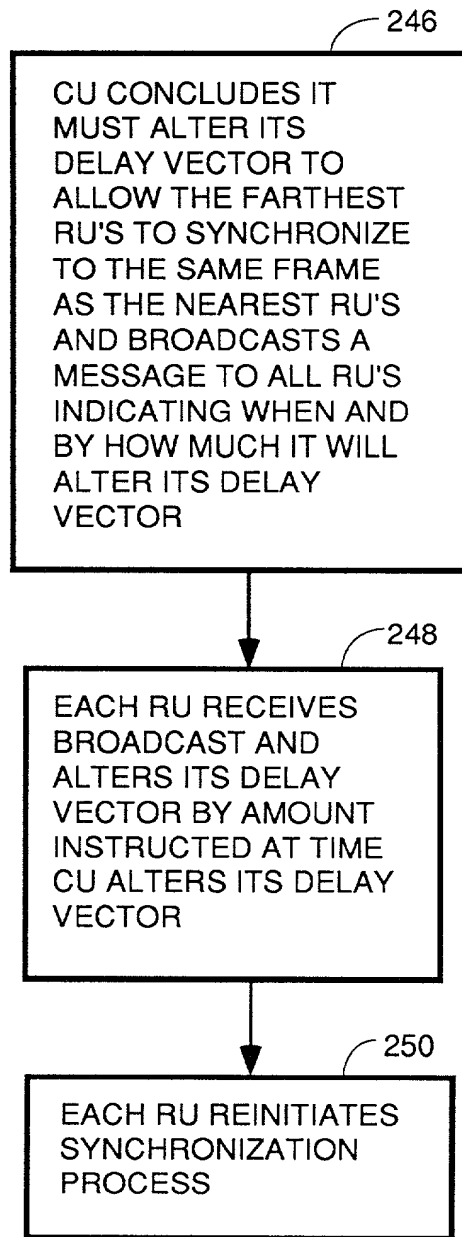


FIG. 5C

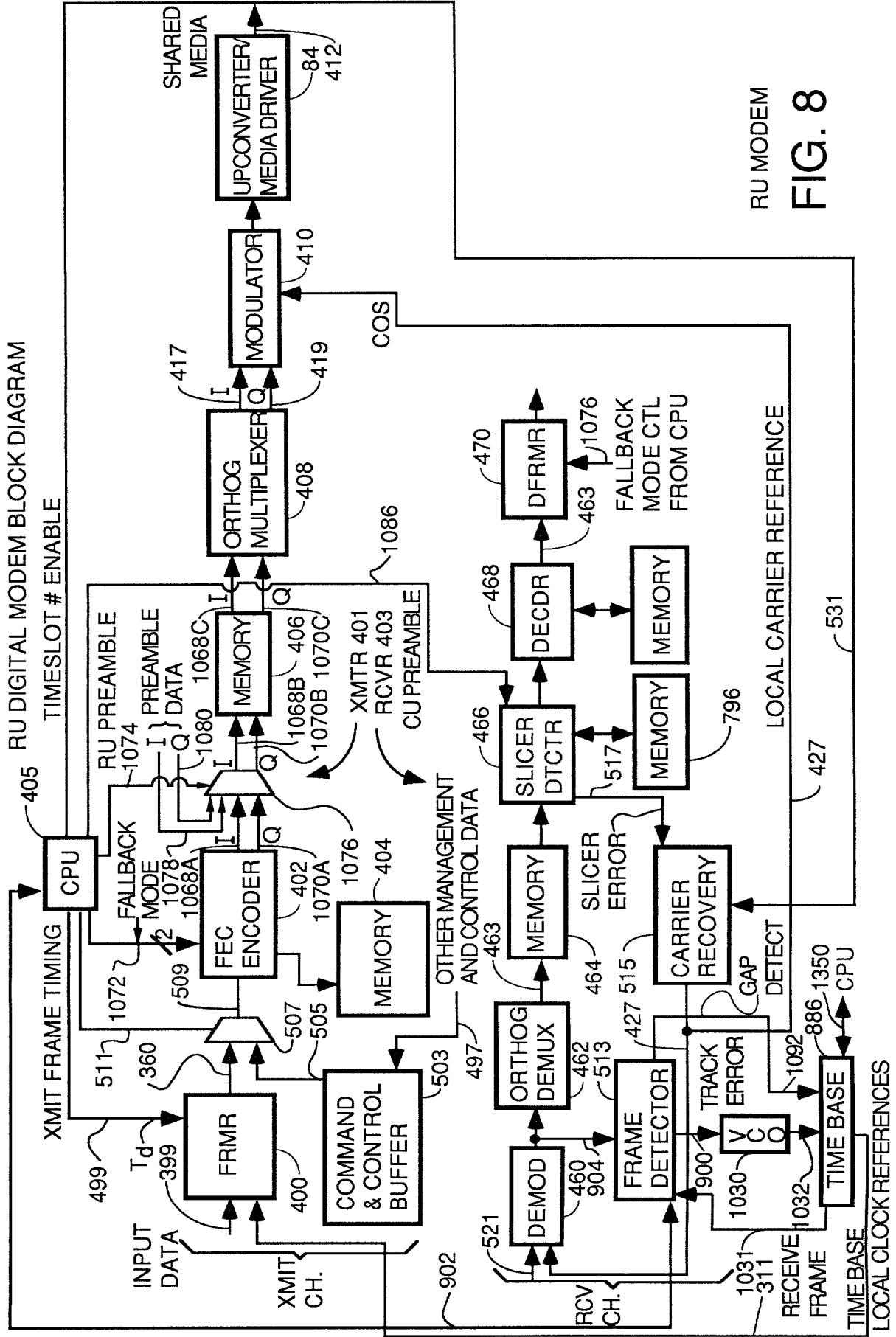


**FIG. 6**  
DEAD RECKONING RE-SYNC





**FIG. 7**  
PRECURSOR EMBODIMENT



RU MODEM  
FIG. 8

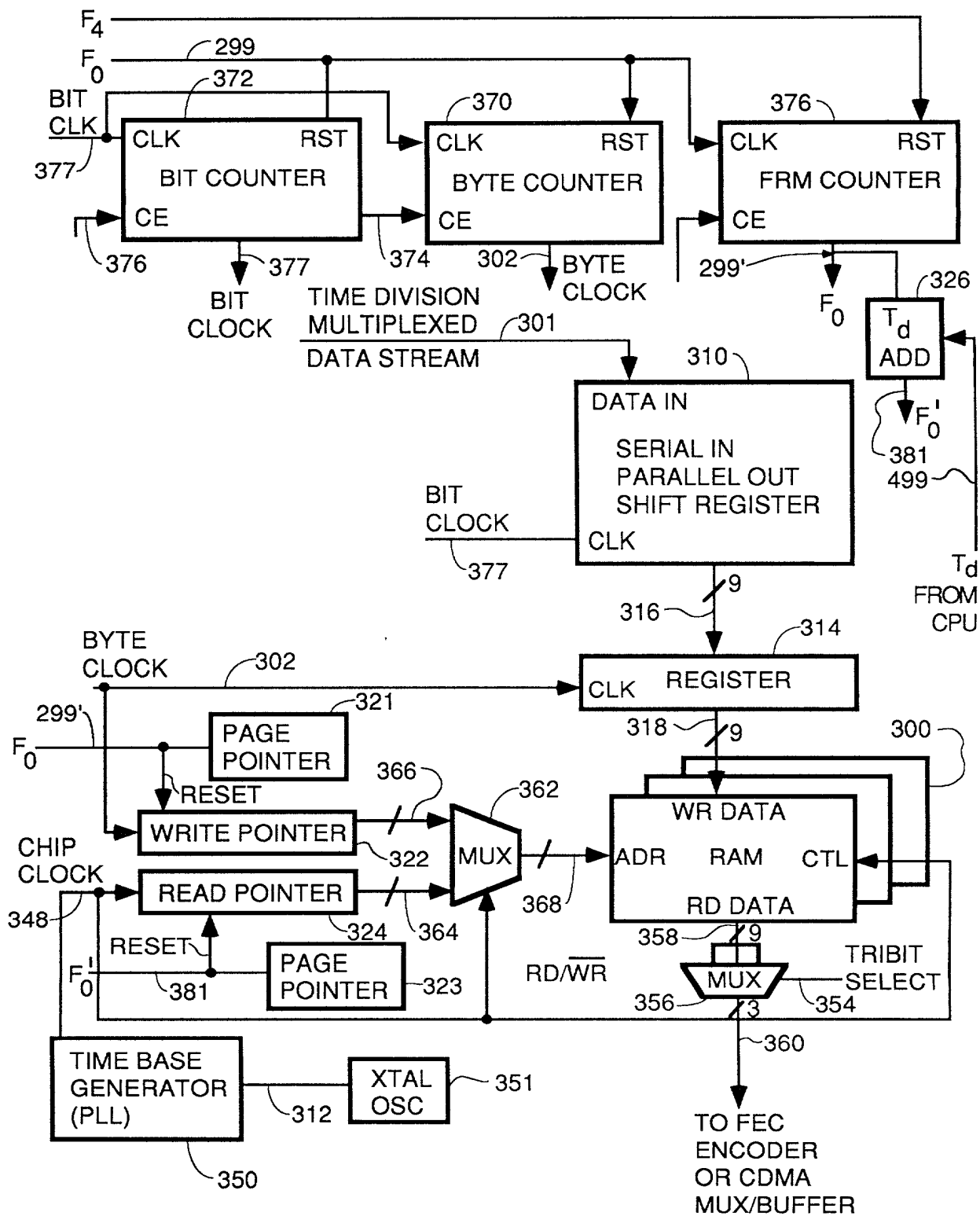


FIG. 9

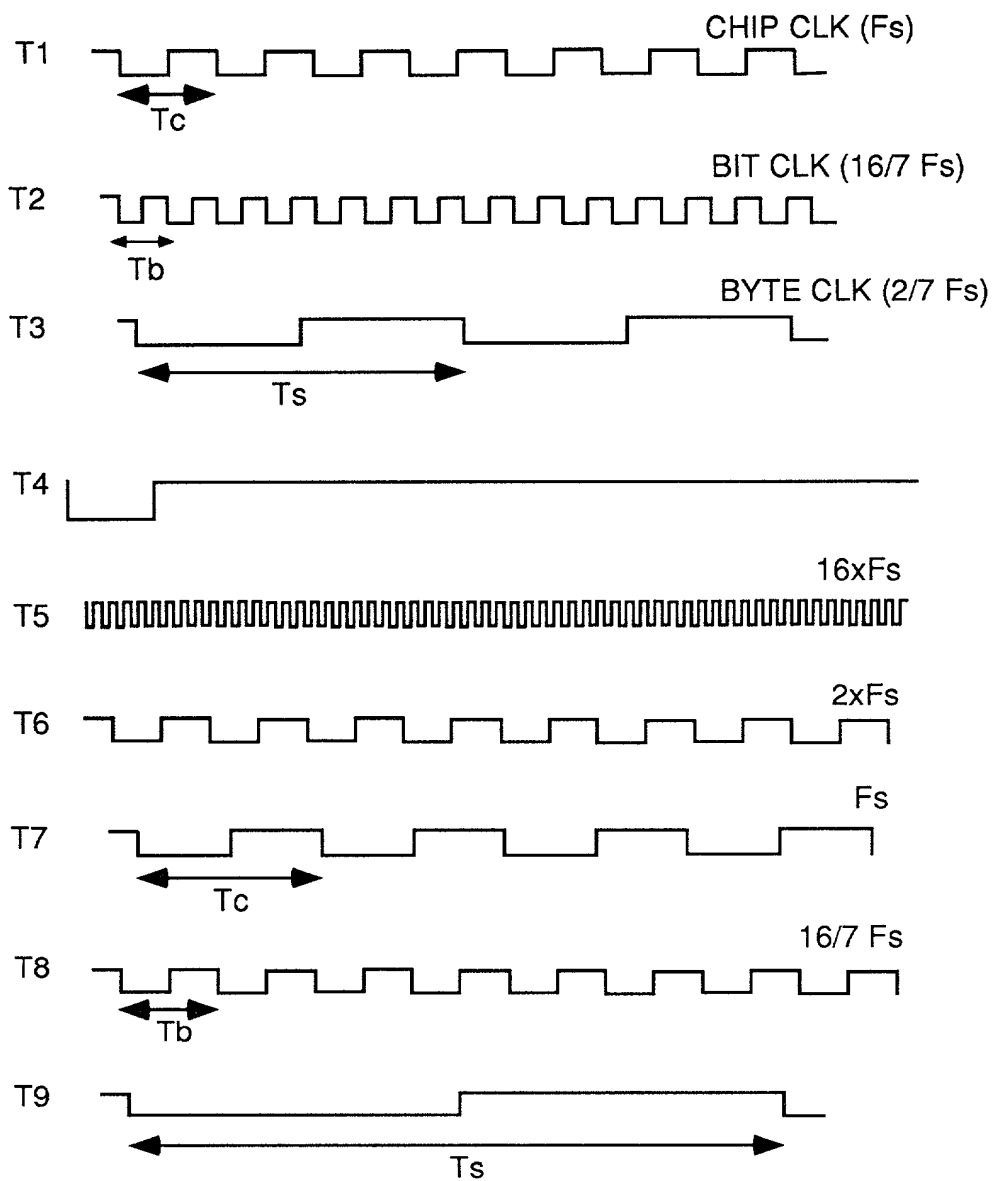
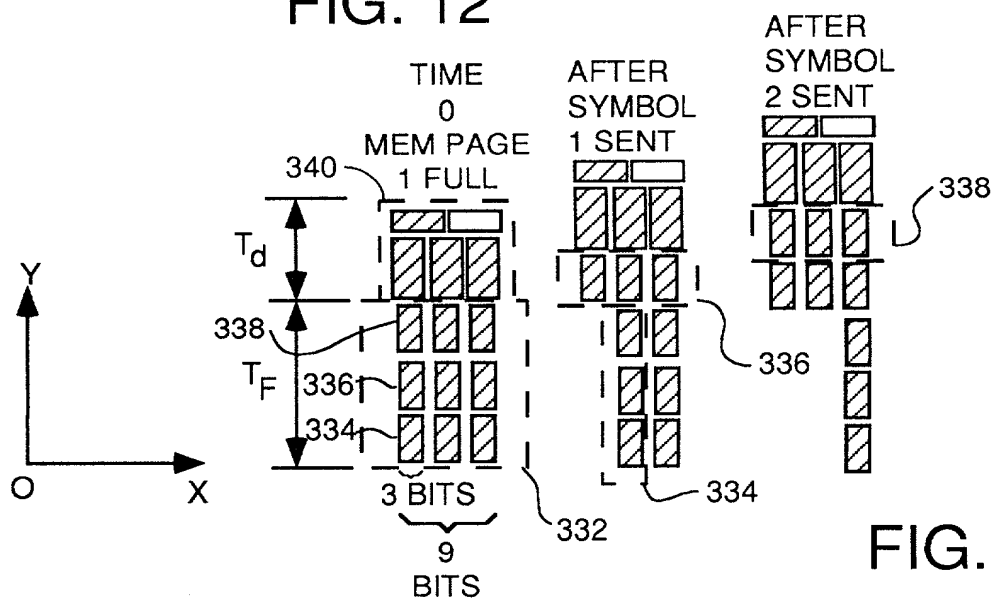
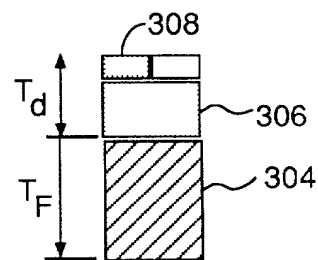
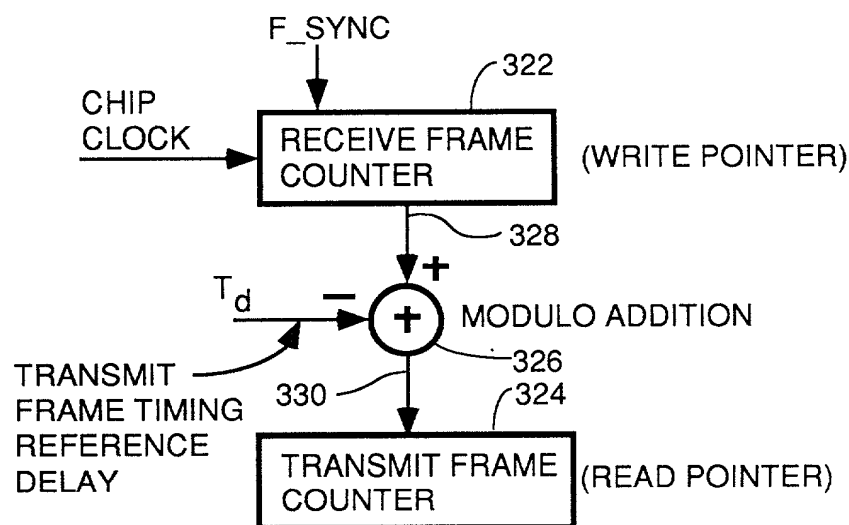


FIG. 10



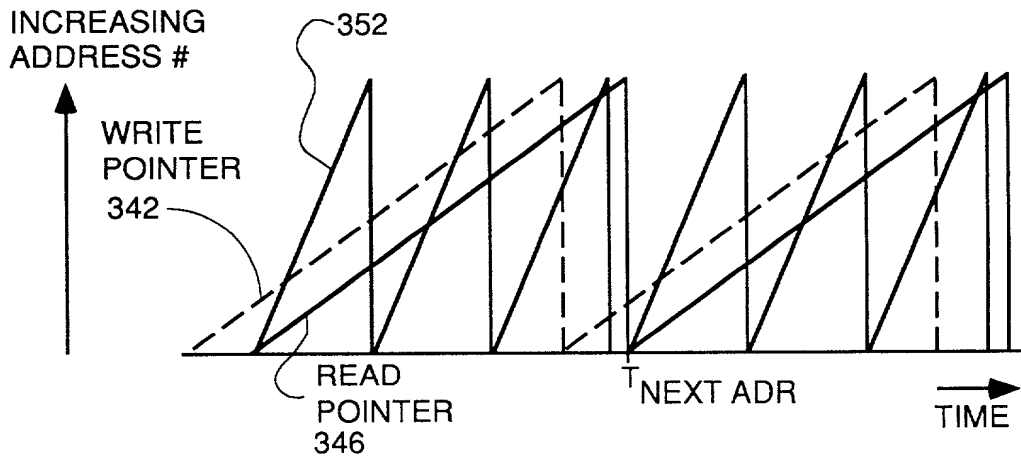


FIG. 15

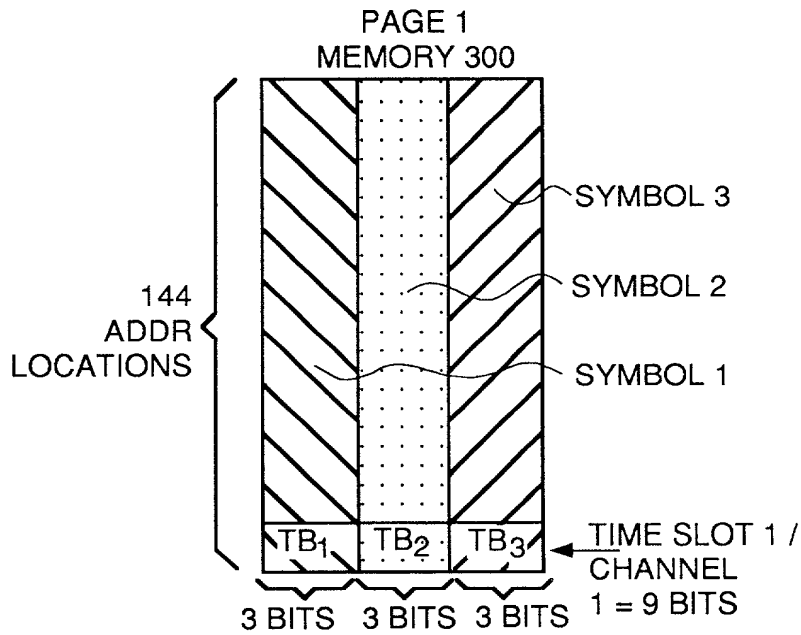
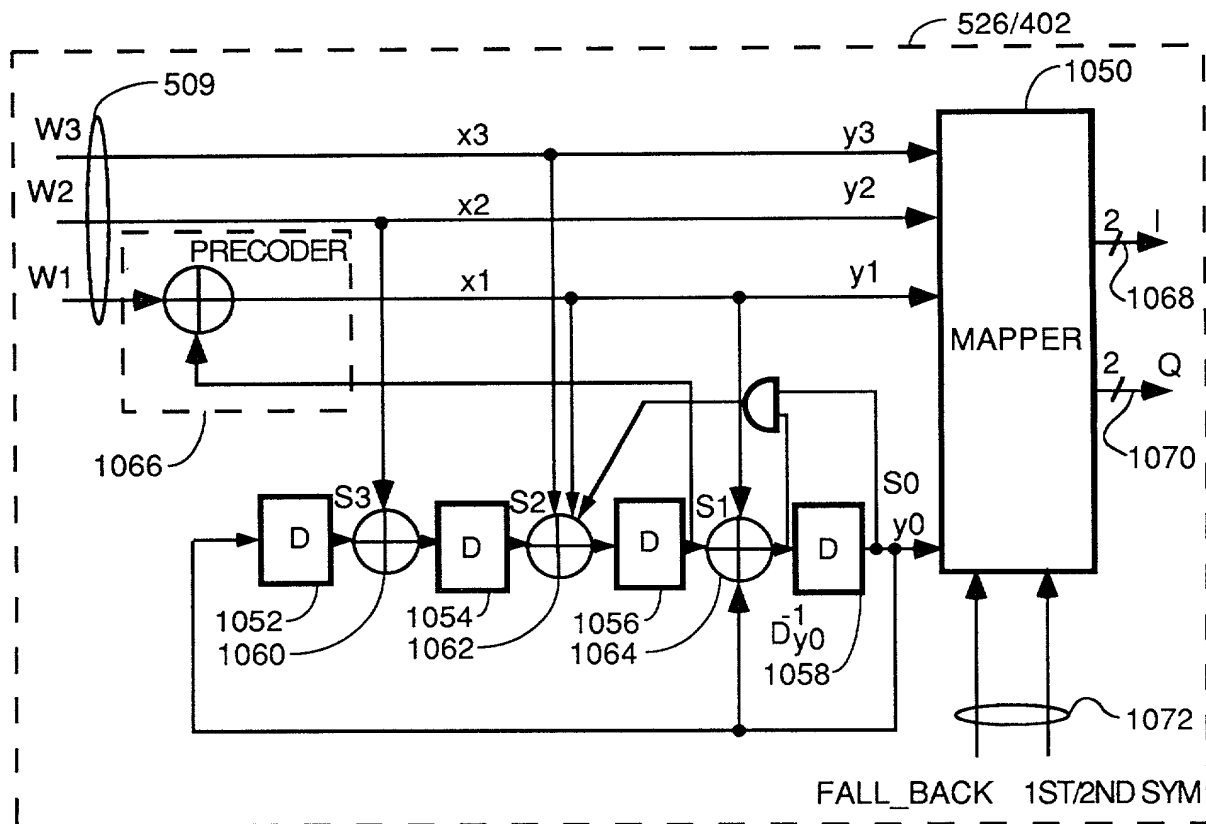


FIG. 16



PREFERRED TRELLIS ENCODER

FIG. 17





INFORMATION  
VECTOR [B]  
FOR EACH  
SYMBOL

ORTHOGONAL  
CODE MATRIX

$$\begin{array}{c} 483 \\ 481 \end{array} \begin{bmatrix} 0 & 1 & 1 & 0 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 0 & 1 \\ 0 & 1 & 0 & 0 \\ \vdots & & & \end{bmatrix} \times \begin{bmatrix} C_{1,1} & C_{1,2} & \cdots & C_{1,144} \\ C_{2,1} & C_{2,2} & \cdots & C_{2,144} \\ \vdots & \vdots & & \vdots \end{bmatrix}$$

FIG. 20A

$$\begin{array}{c} \text{REAL} \\ \text{PART OF} \\ \text{INFO} \\ \text{VECTOR} \\ \text{[b]} \text{ FOR} \\ \text{FIRST} \\ \text{SYMBOL} \end{array} \begin{array}{c} 405 \\ \begin{bmatrix} +3 \\ -1 \\ -1 \\ +3 \end{bmatrix} \end{array} \cdot \begin{array}{c} \begin{bmatrix} 1 & 1 & 1 & 1 \\ -1 & -1 & 1 & 1 \\ -1 & 1 & -1 & 1 \\ -1 & 1 & 1 & -1 \end{bmatrix} \\ 407 \end{array} = \begin{array}{c} \begin{bmatrix} 4 \\ 0 \\ 0 \\ -8 \end{bmatrix} \\ 409 \end{array}$$

REAL PART OF  
RESULT  
VECTOR

$$\begin{bmatrix} b_{\text{REAL}} \end{bmatrix} \times \begin{bmatrix} \text{CODE MATRIX} \end{bmatrix} = \begin{bmatrix} R_{\text{REAL}} \end{bmatrix} = \text{"CHIPS OUT" ARRAY-REAL}$$

FIG. 20B

MAPPING FOR FALL-BACK MODE - LSB'S

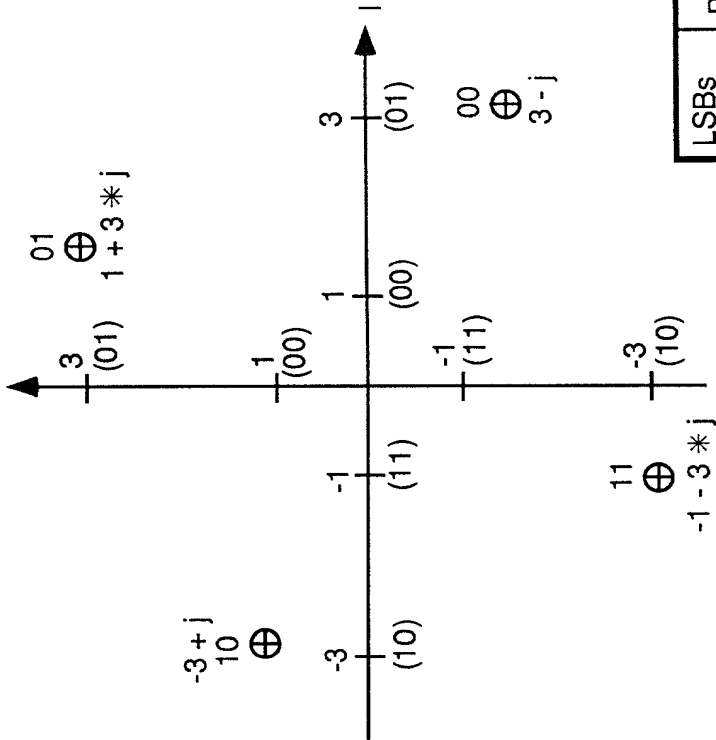


FIG. 21

MSBs y3 y2	PHASE difference (2nd-1st symbol)	1+jQ WHEN LSB=00	1+jQ WHEN LSB=01	1+jQ WHEN LSB=10	1+jQ WHEN LSB=11
00	0	3-j	1+j3	-3+j	-1-j3
01	90	1+j3	-3+j	-1-j3	3-j
10	180	-3+j	-1-j3	3-j	1+j3
11	-90	-1-j3	3-j	1+j3	-3+j

LSBs y1 y0	PHASE	1+jQ
00	0	3-j
01	90	1+j3
10	180	-3+j
11	-90	-1-j3

LSB & MSB FALLBACK MODE MAPPINGS

FIG. 22

FIG. 24

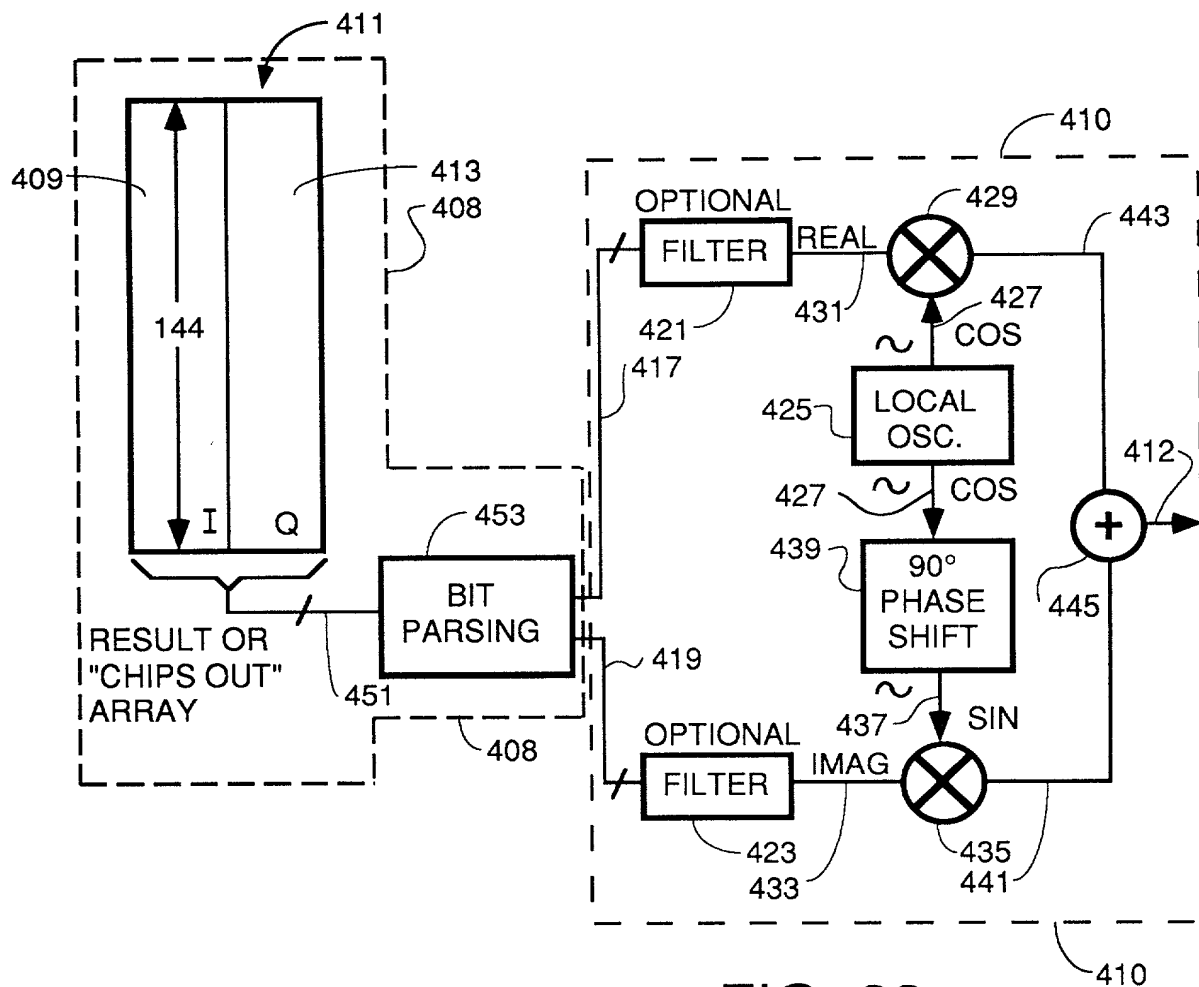


FIG. 23

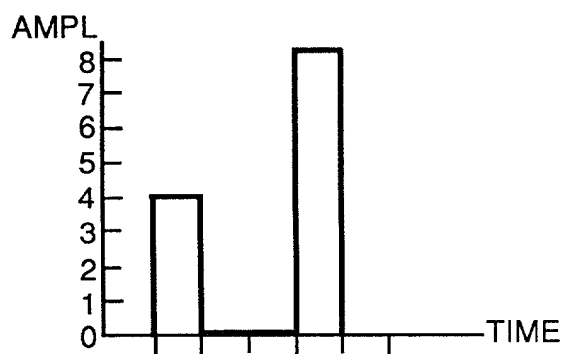


FIG. 24

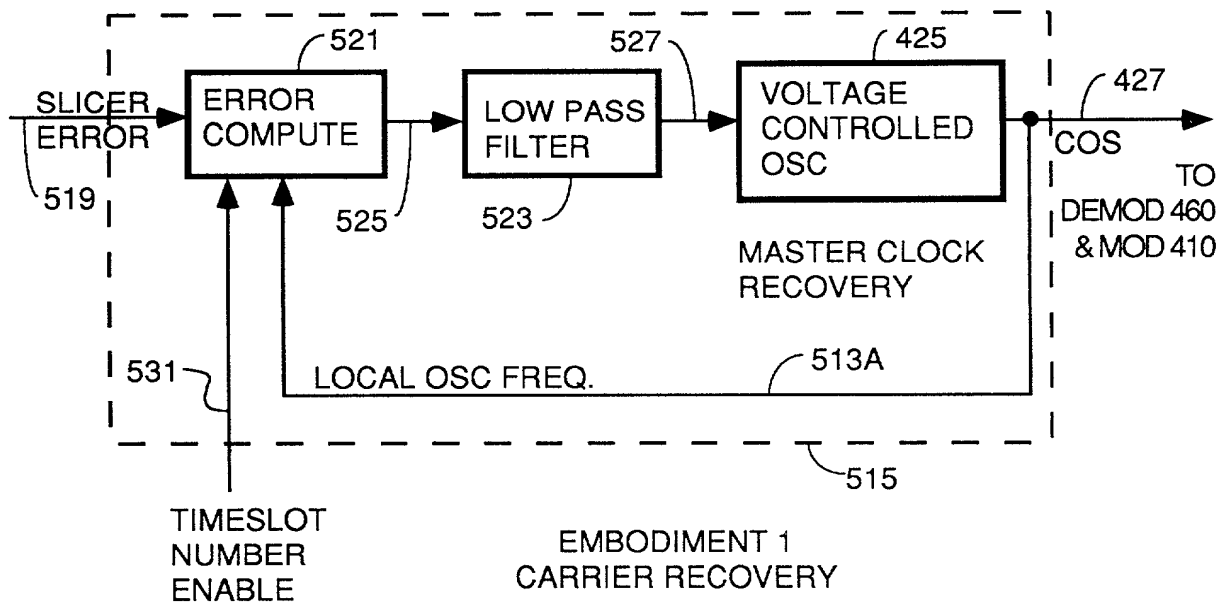


FIG. 25

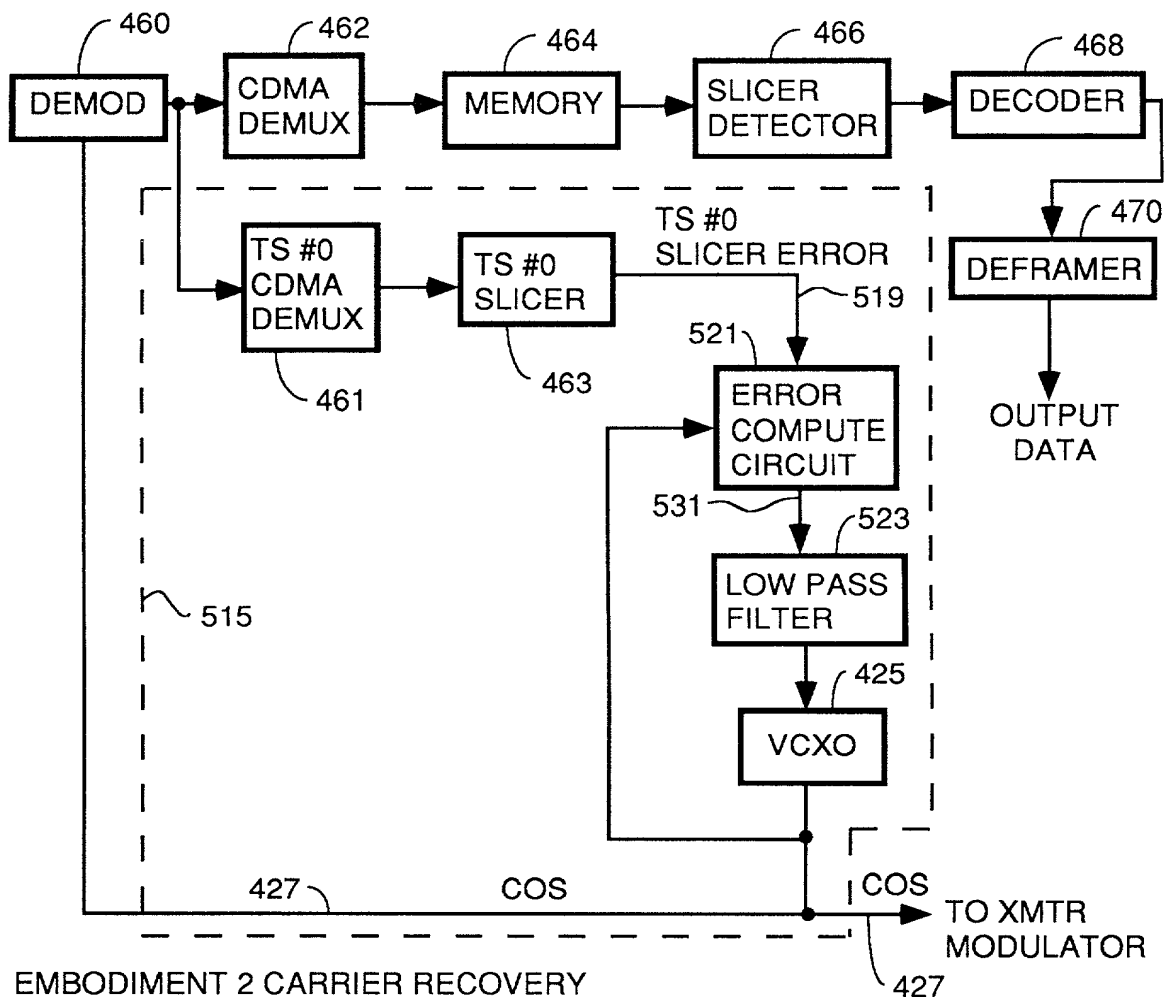


FIG. 26

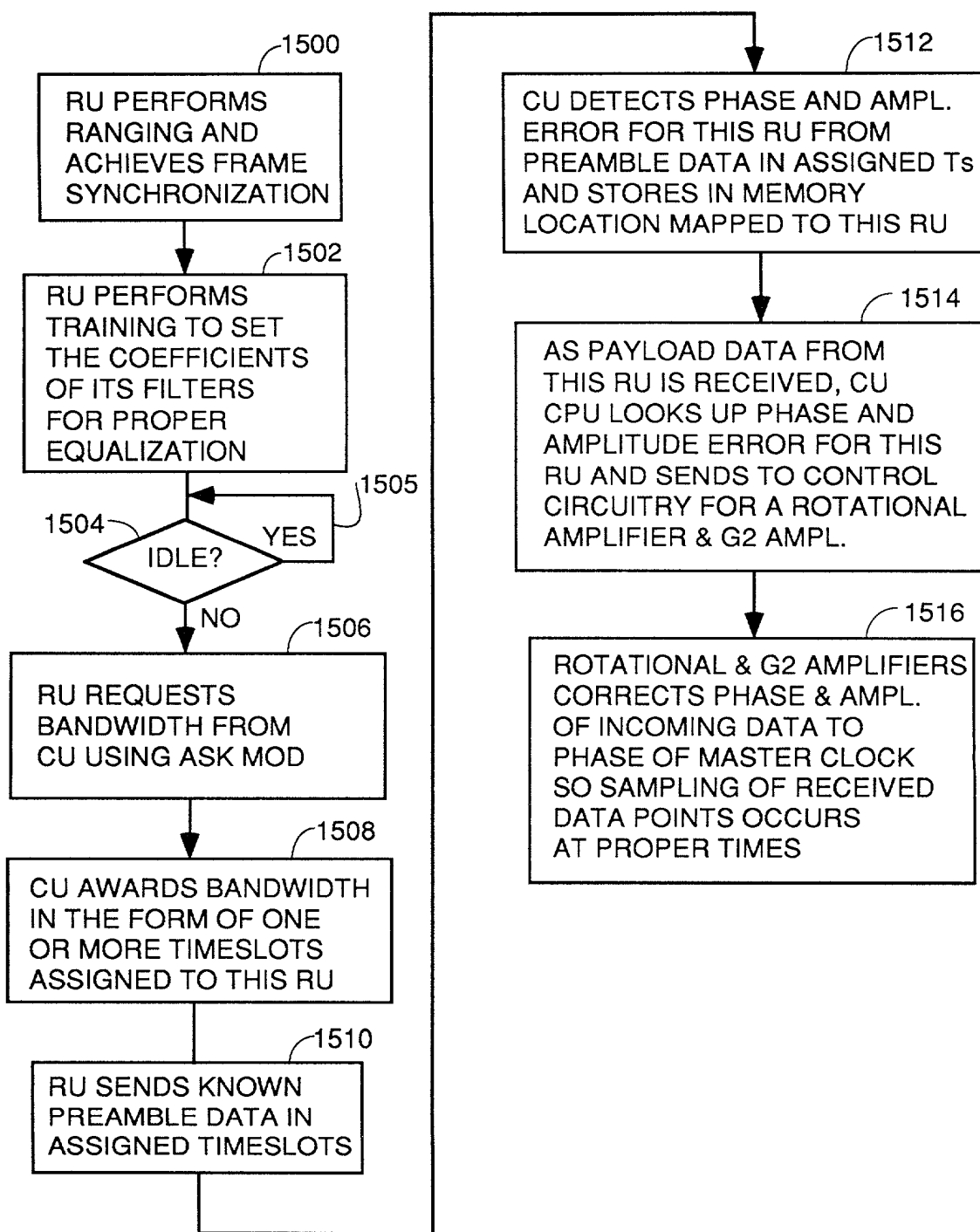
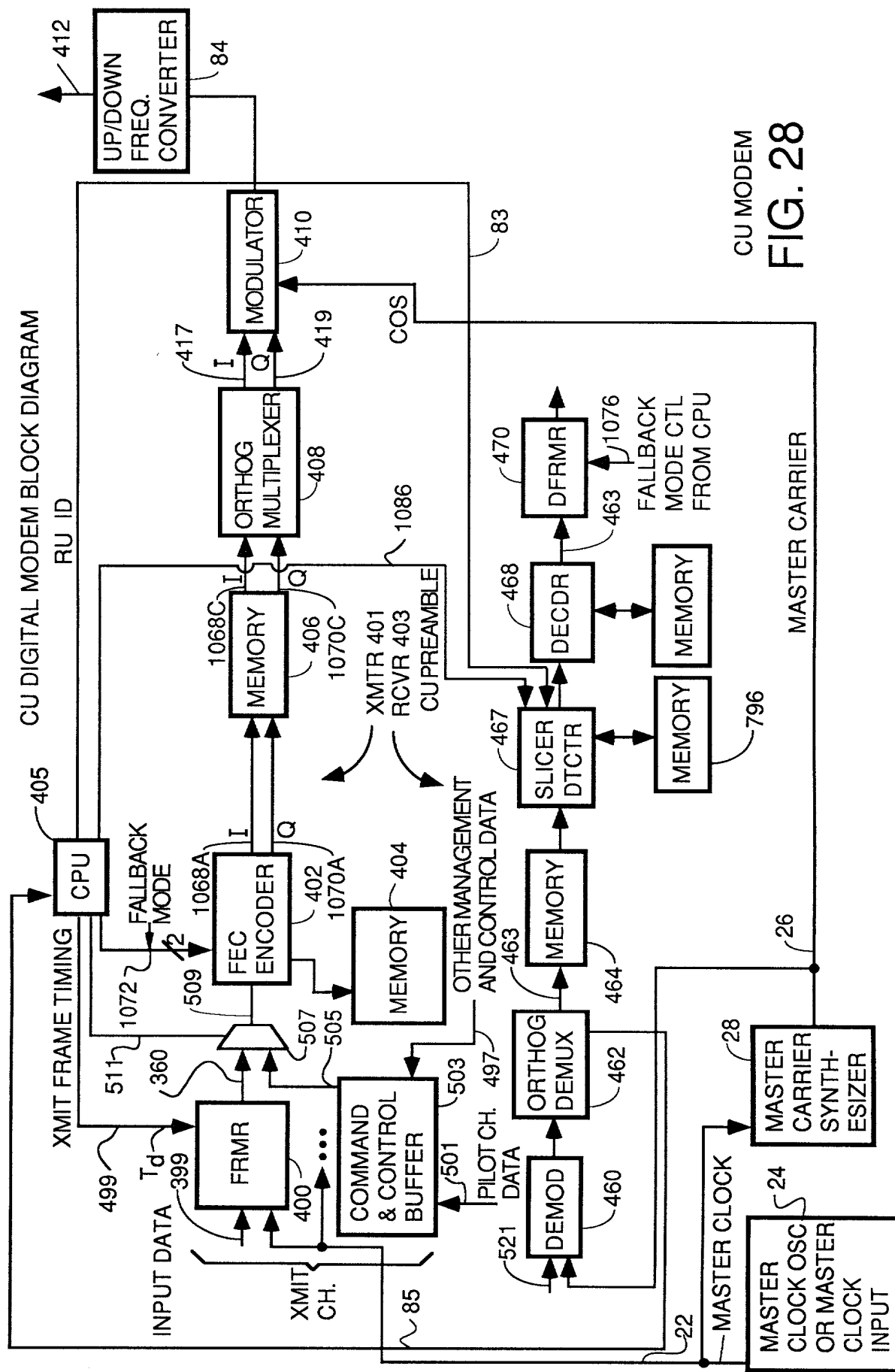


FIG. 27



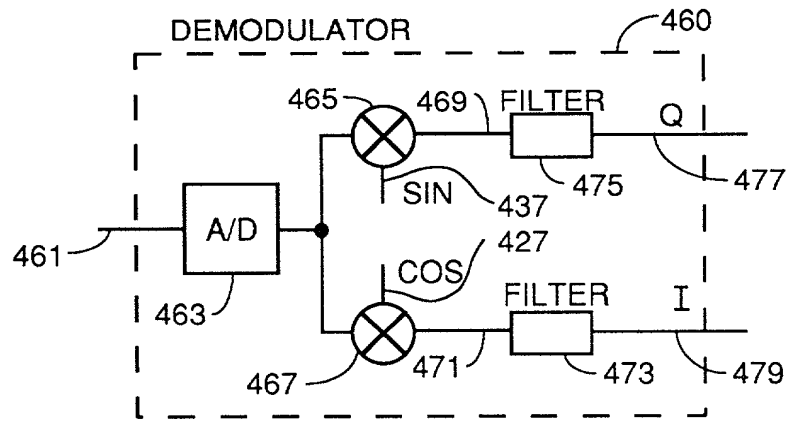


FIG. 29

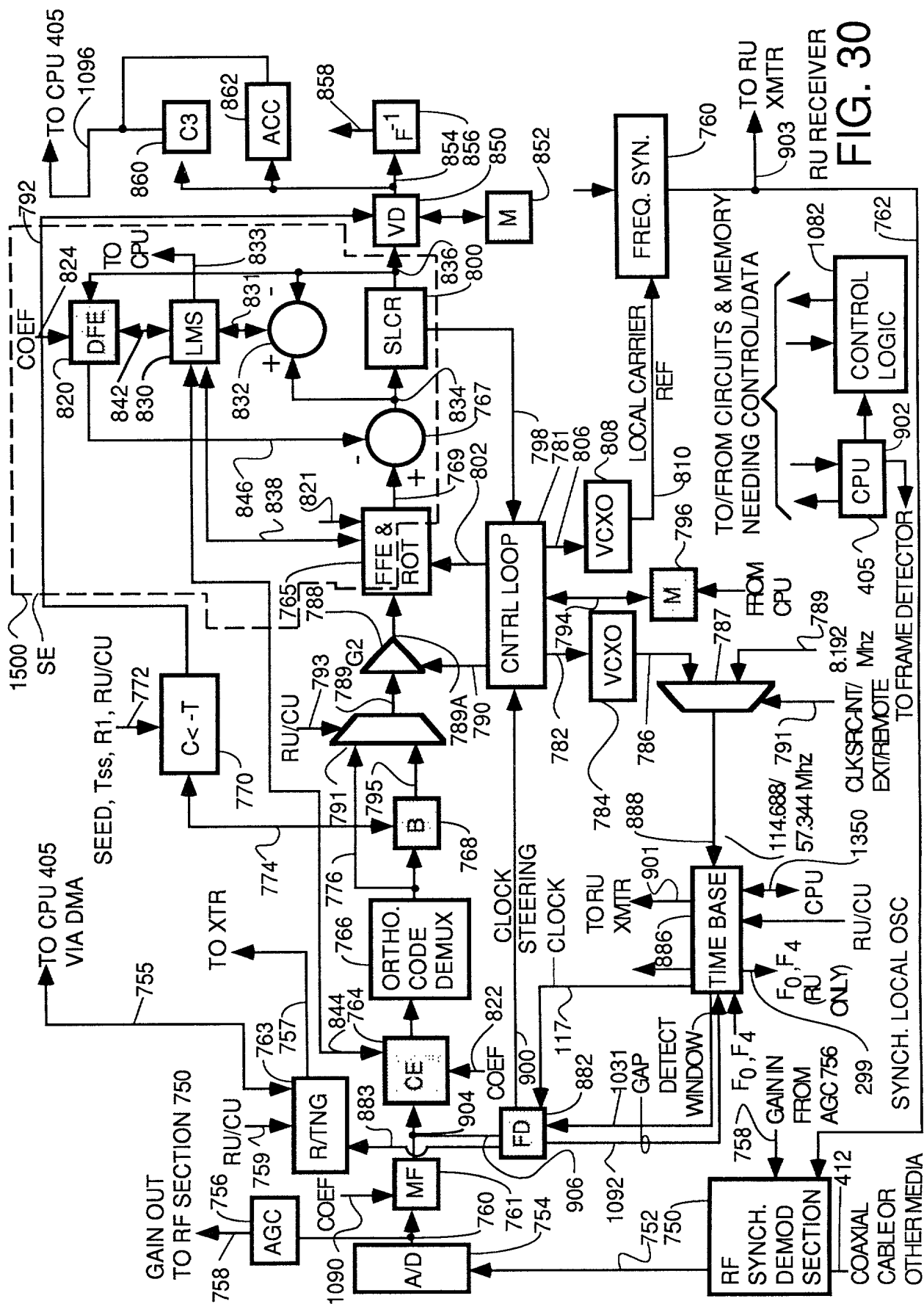
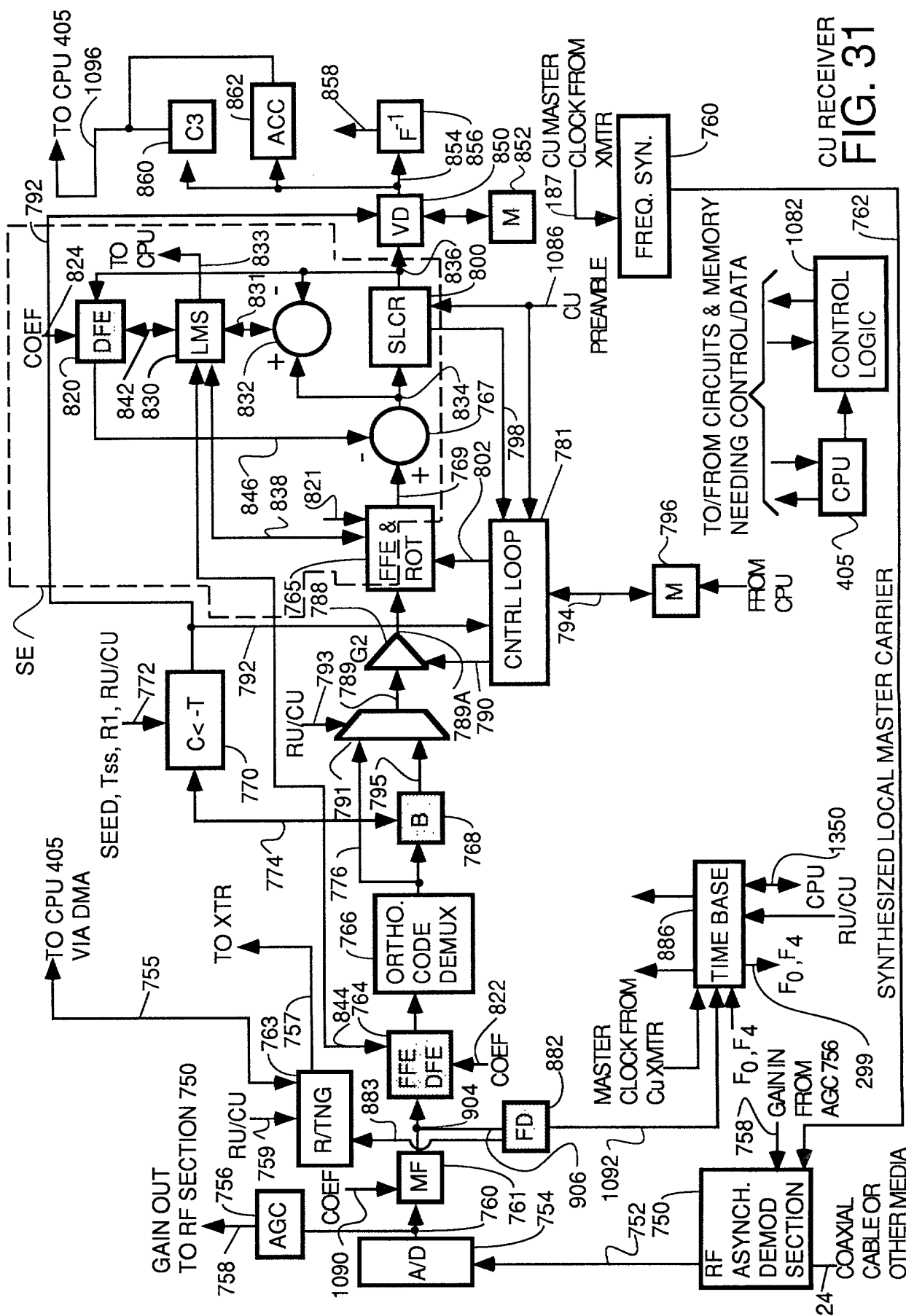
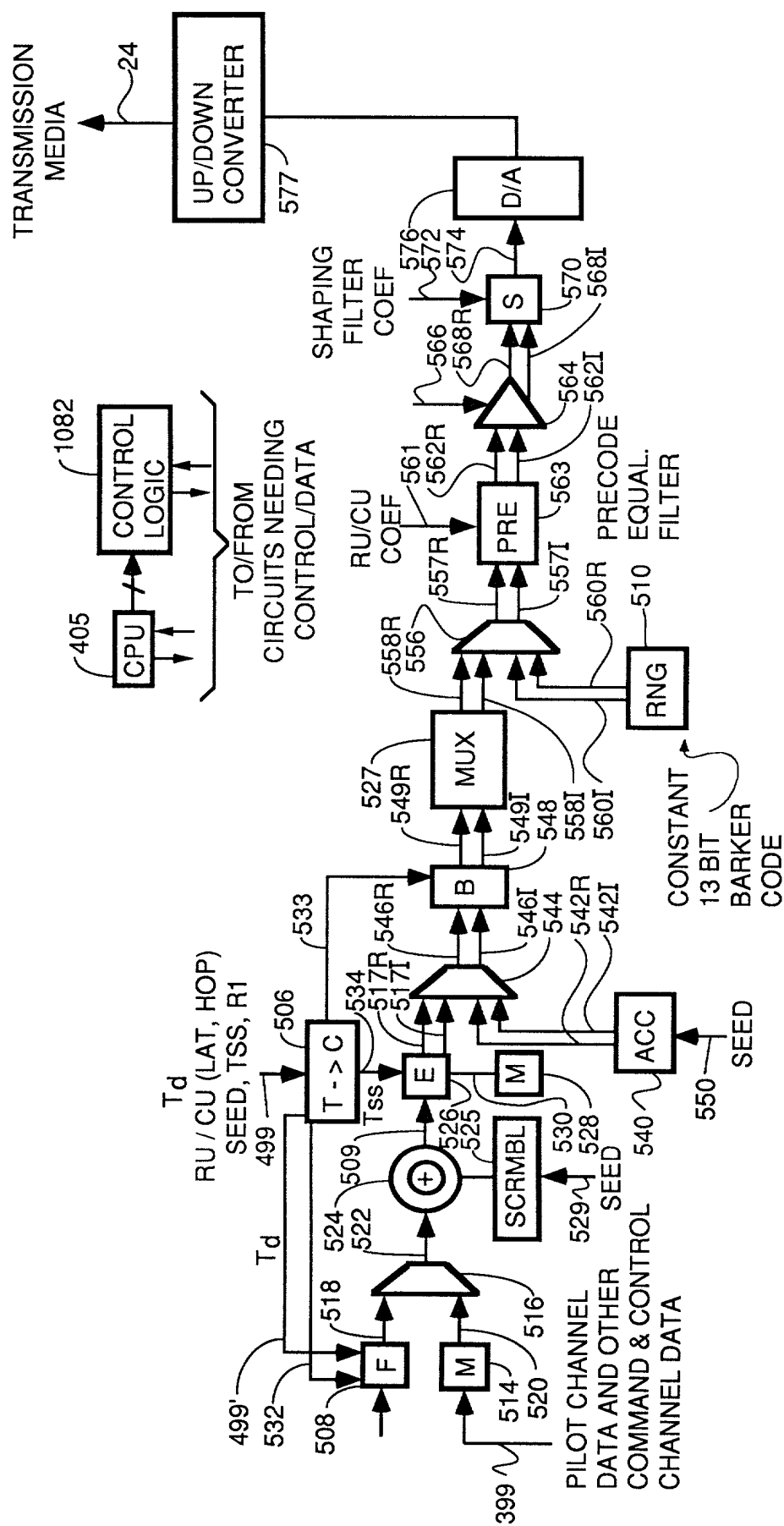


FIG. 30



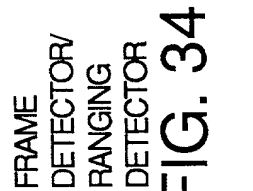




CU TRANSMITTER

FIG. 32





**FIG. 34**

# GAP ACQUISITION TIMING

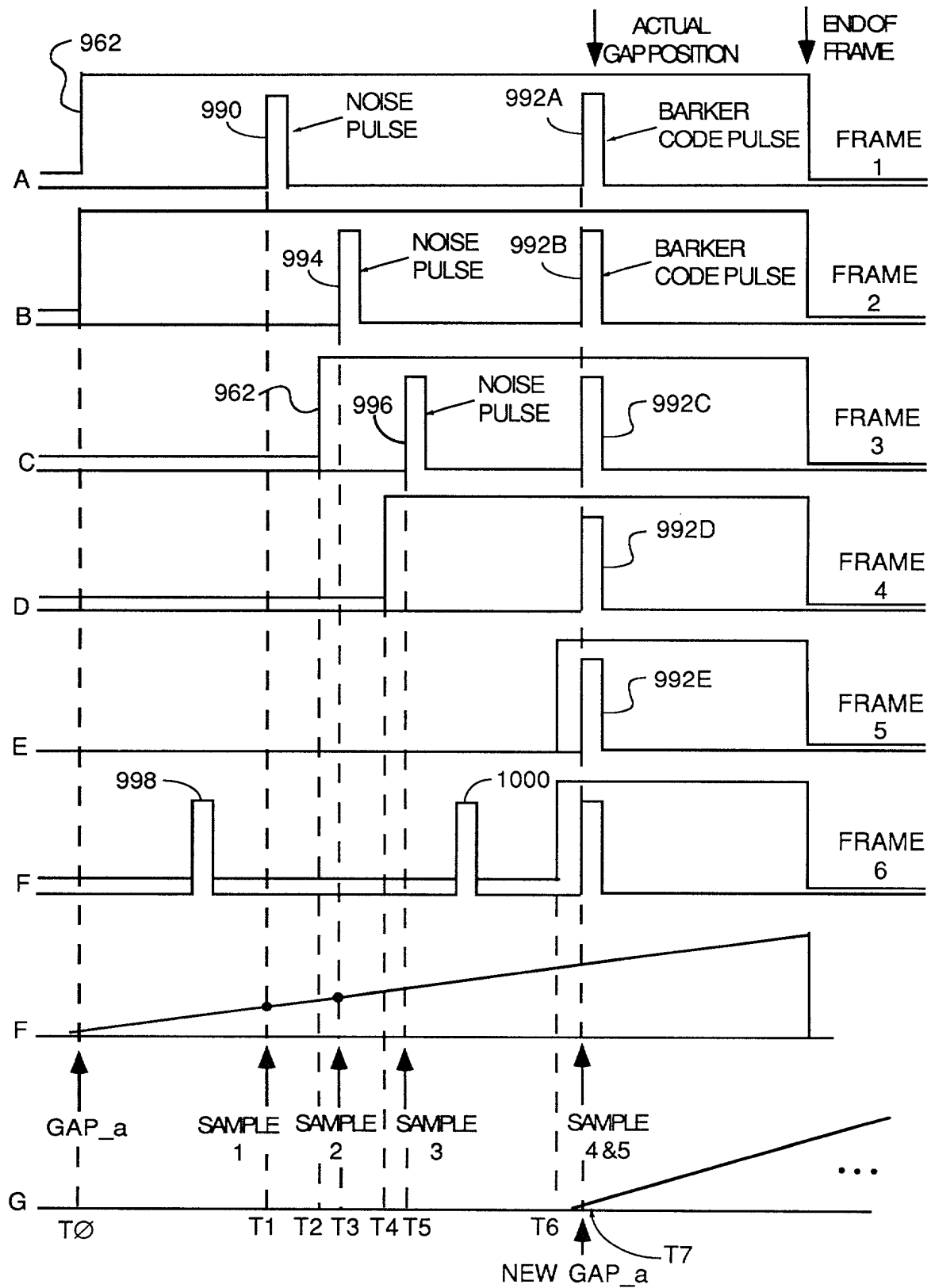


FIG. 35

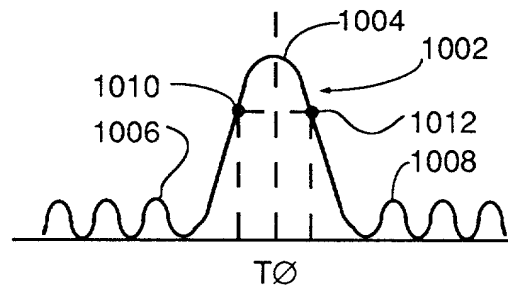


FIG. 36

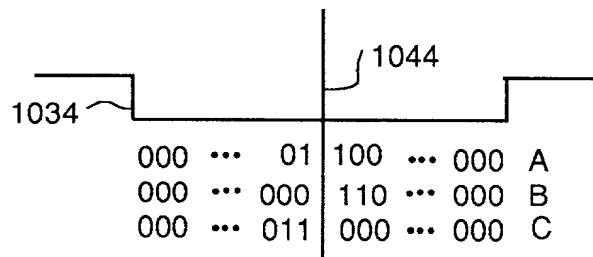


FIG. 37

FINE TUNING TO  
CENTER BARKER CODE

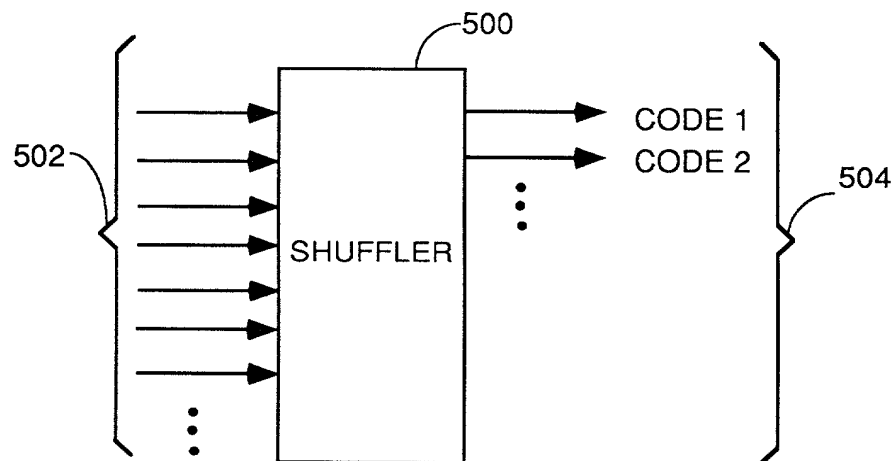


FIG. 38

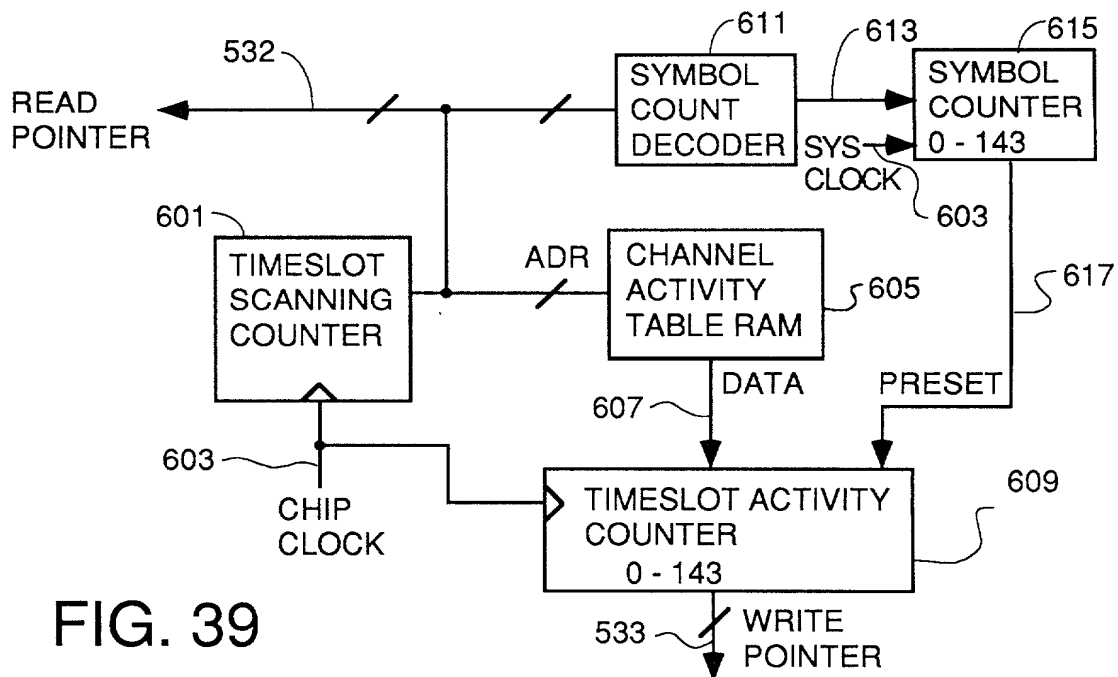


FIG. 39

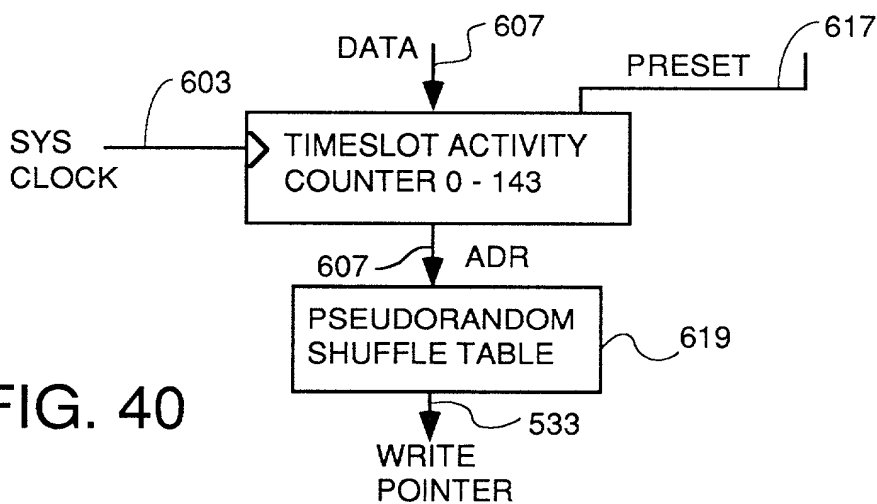


FIG. 40

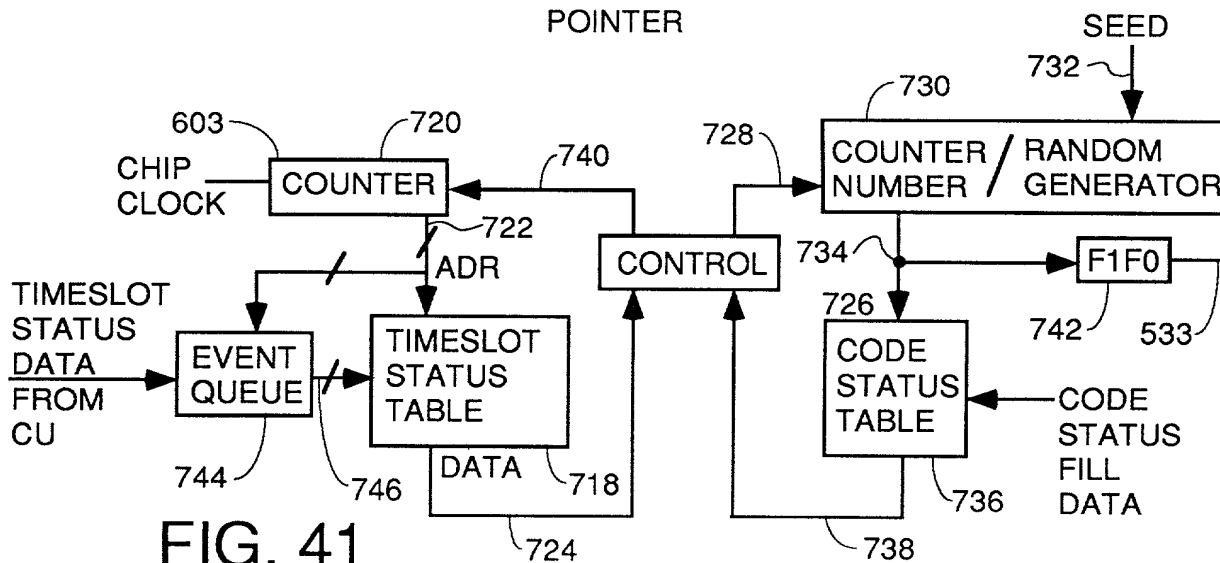


FIG. 41

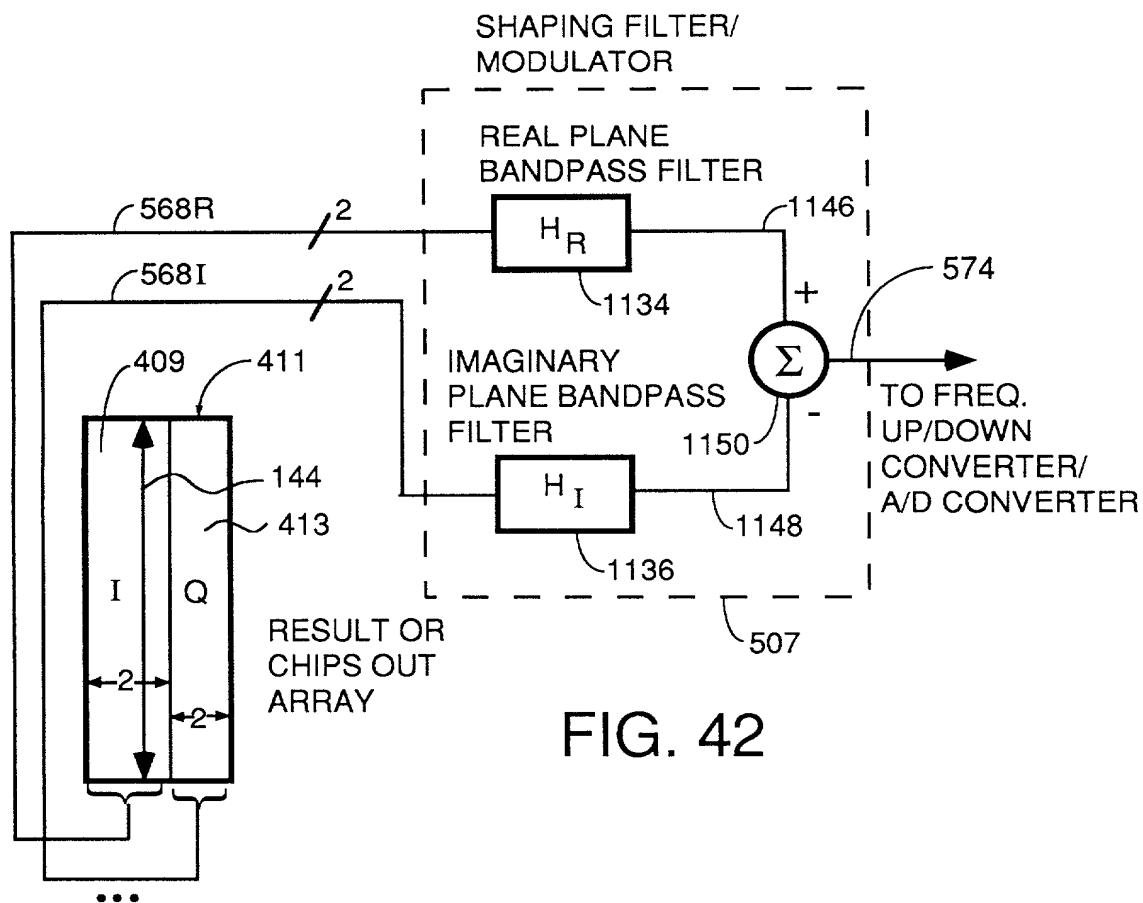


FIG. 42

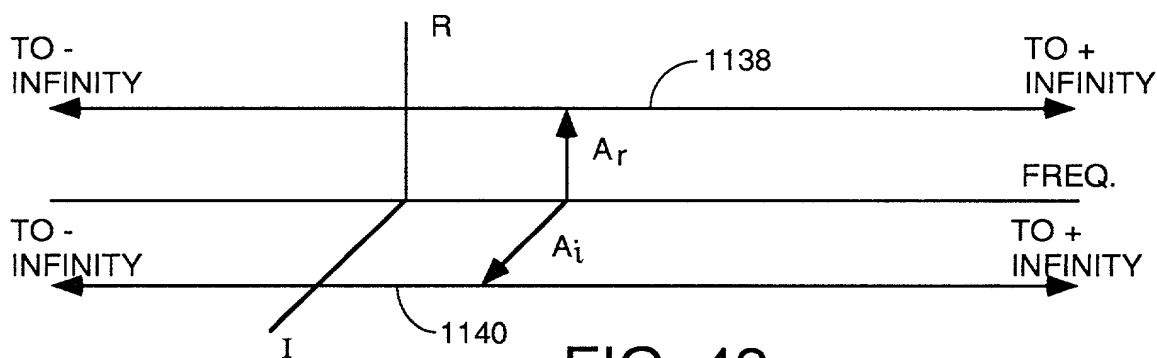


FIG. 43

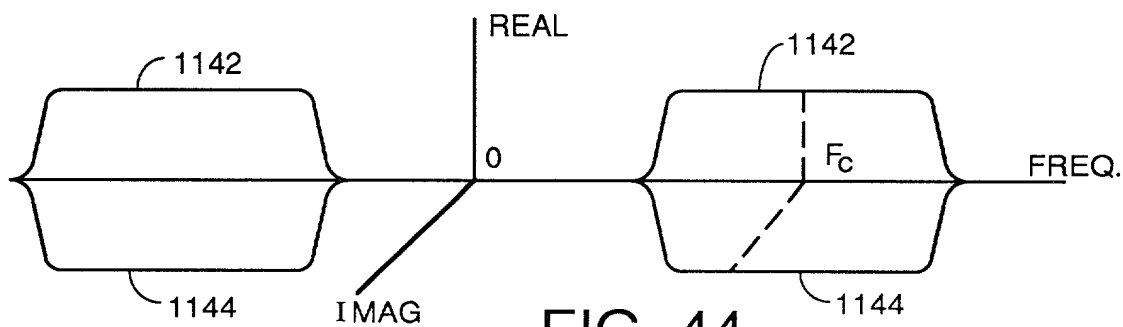
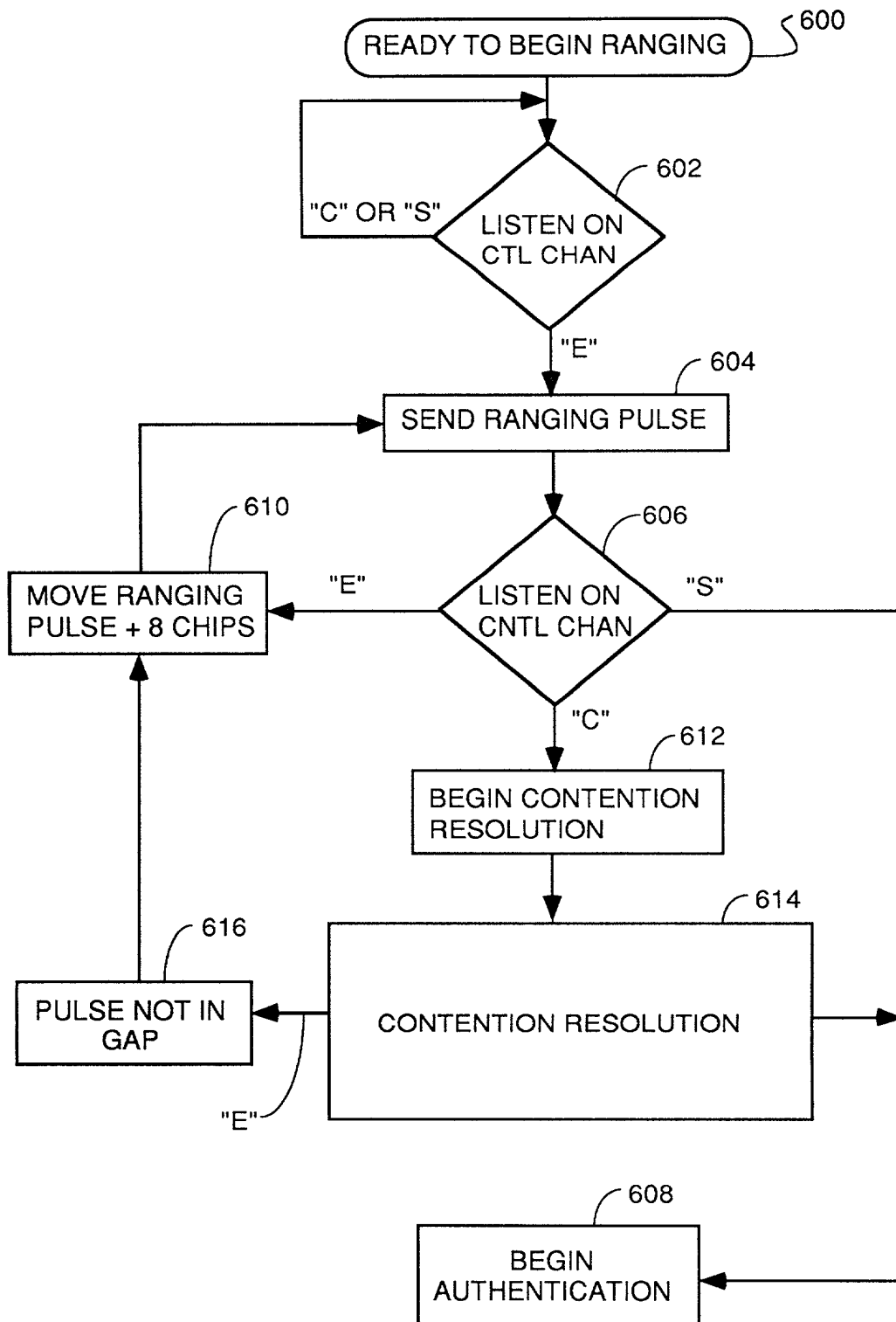


FIG. 44



FIG. 45



RU RANGING  
FIG. 45

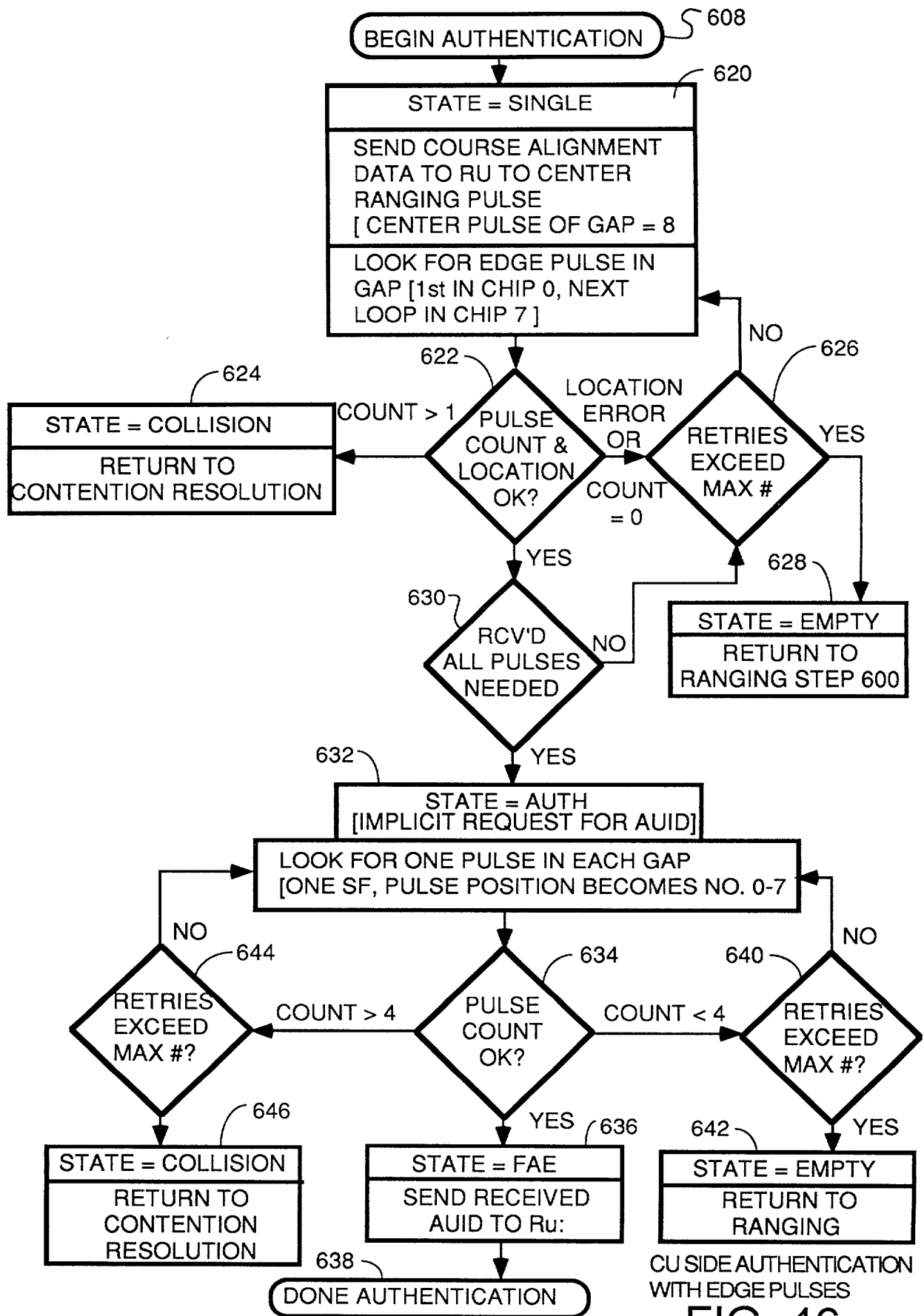
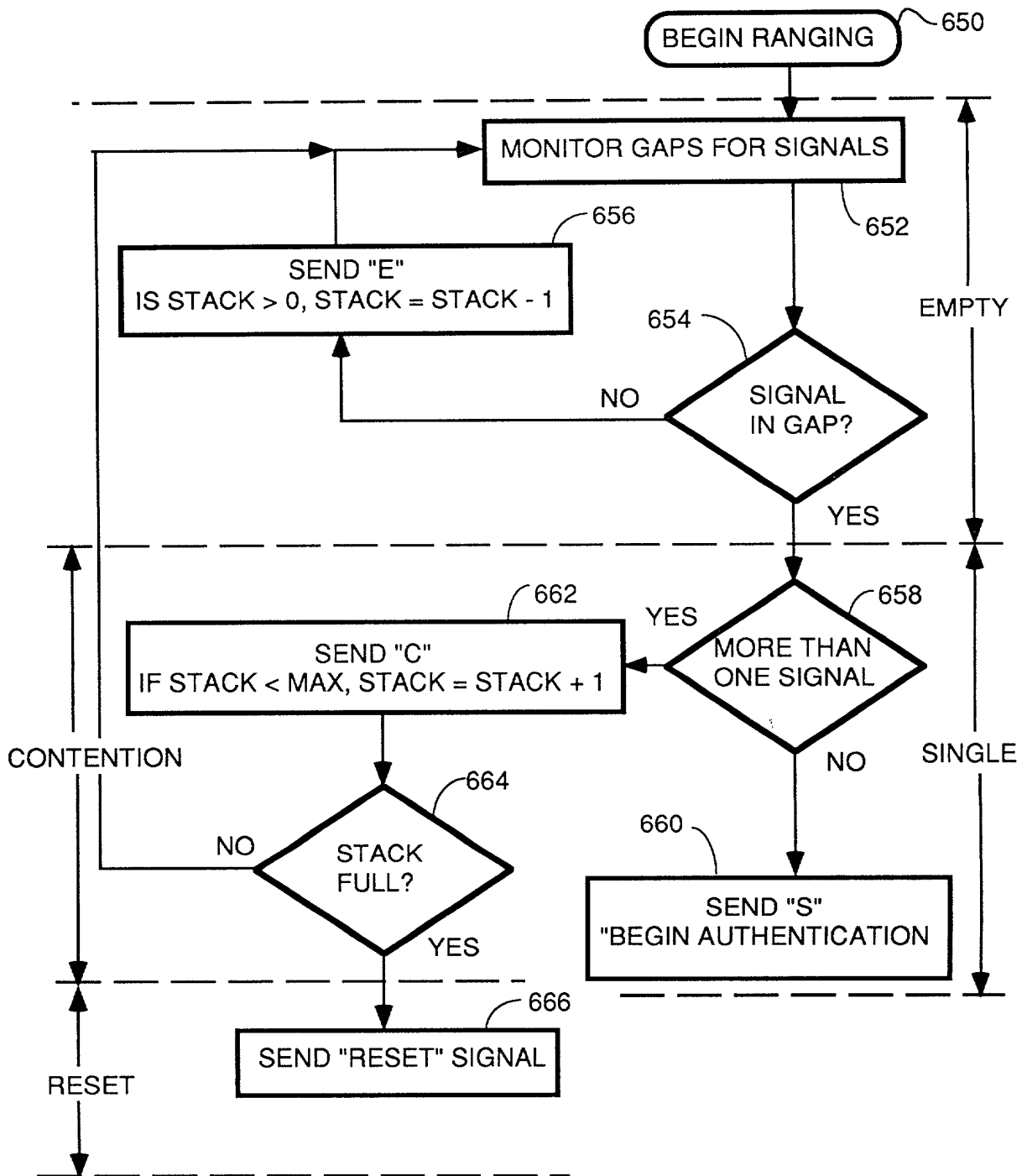
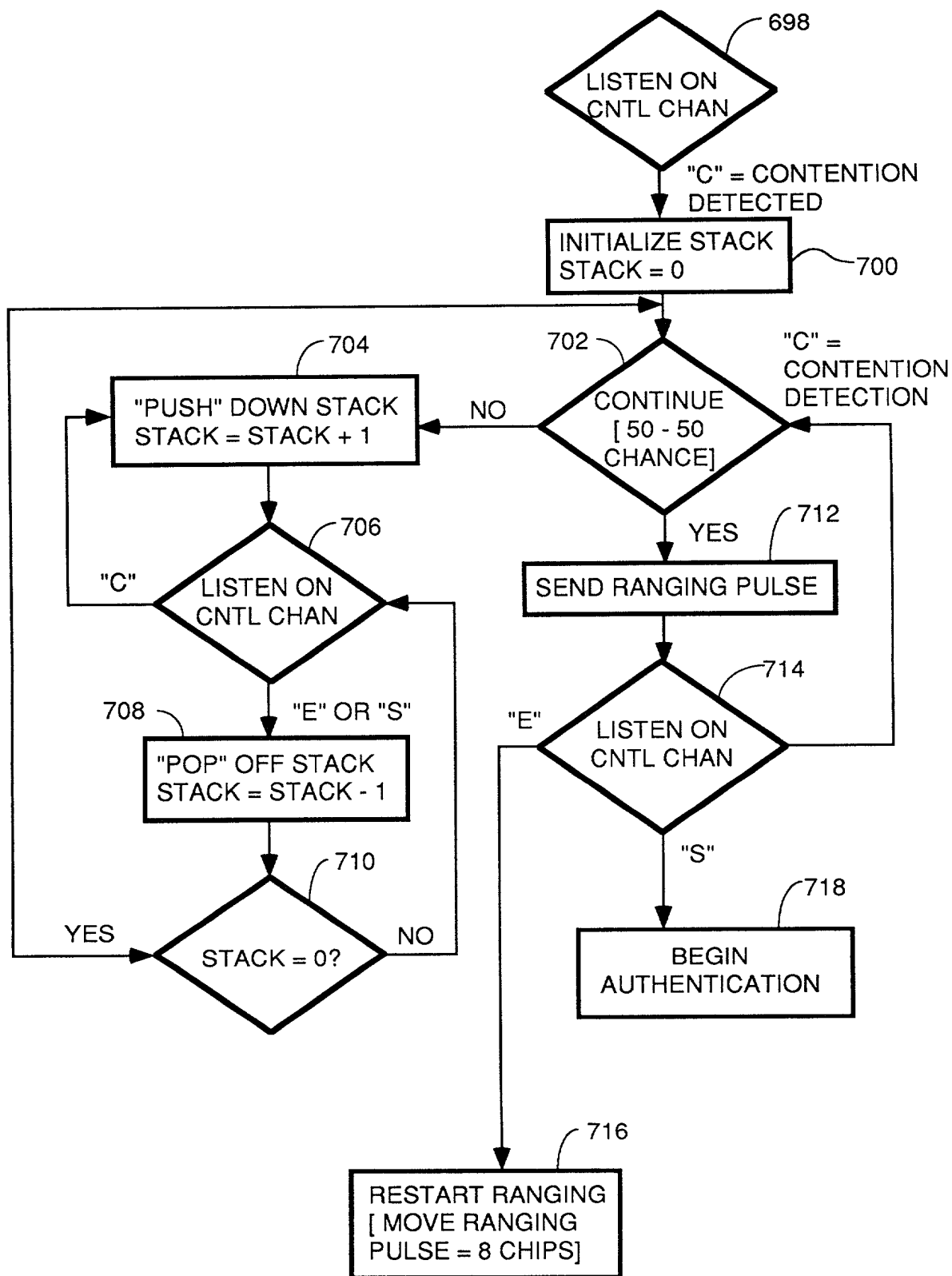


FIG. 46



CU RANGING AND CONTENTION RESOLUTION

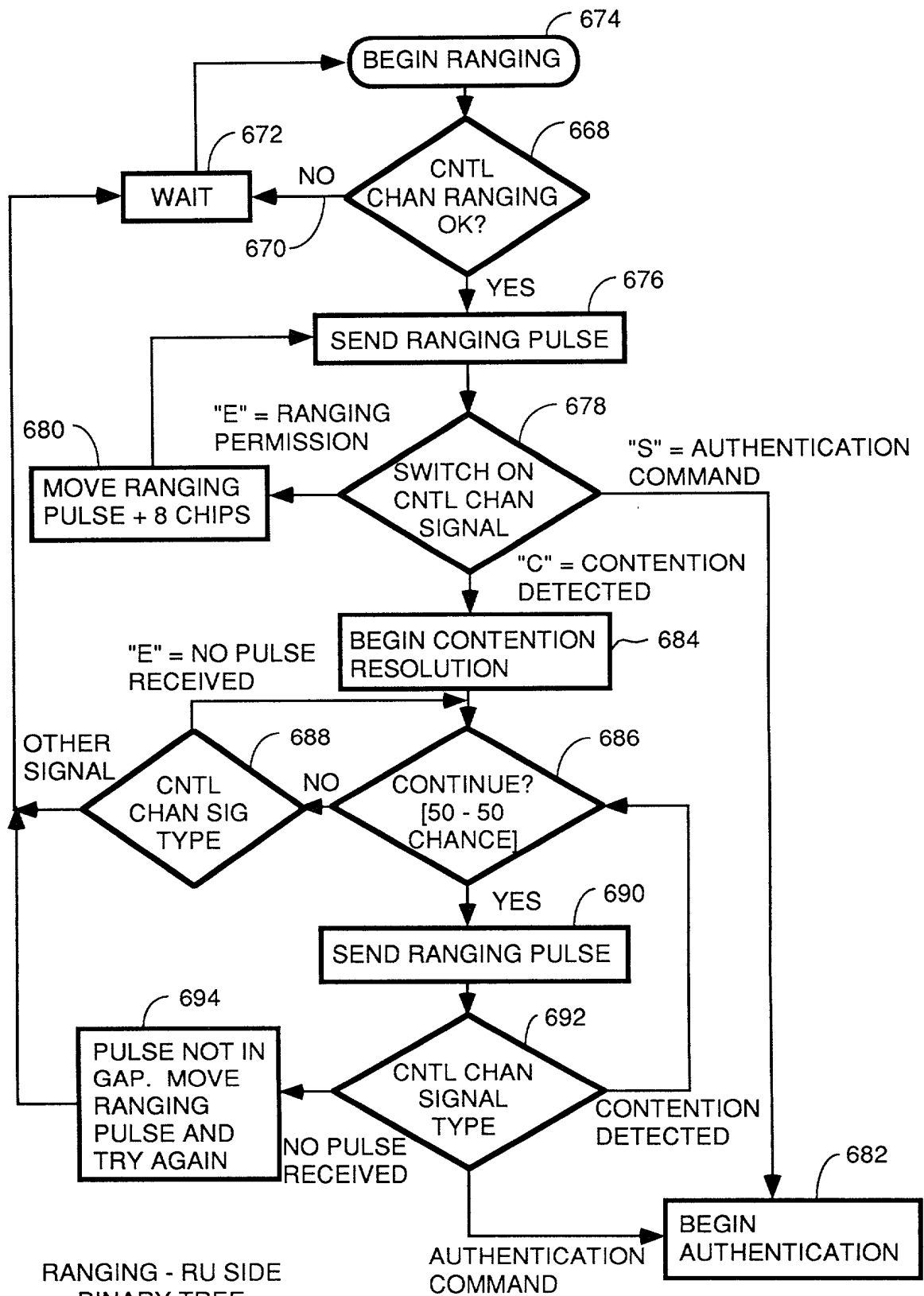
FIG. 47



CONTENTION RESOLUTION - RU  
USING BINARY STACK

FIG. 48

FIG. 49



RANGING - RU SIDE  
BINARY TREE  
ALGORITHM

FIG. 49

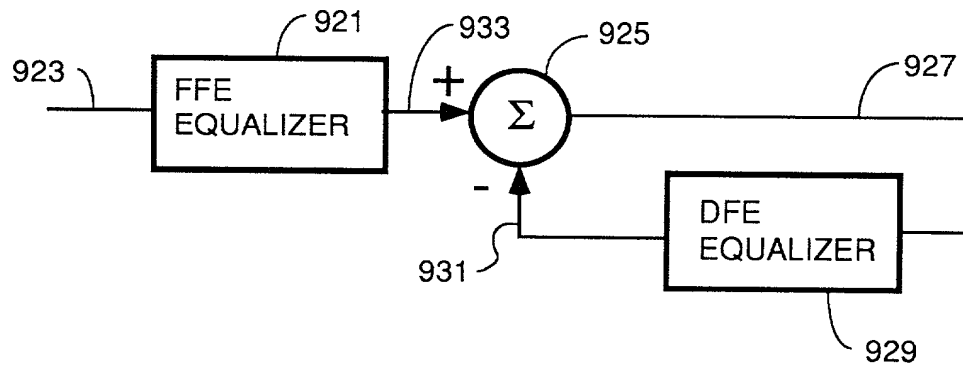
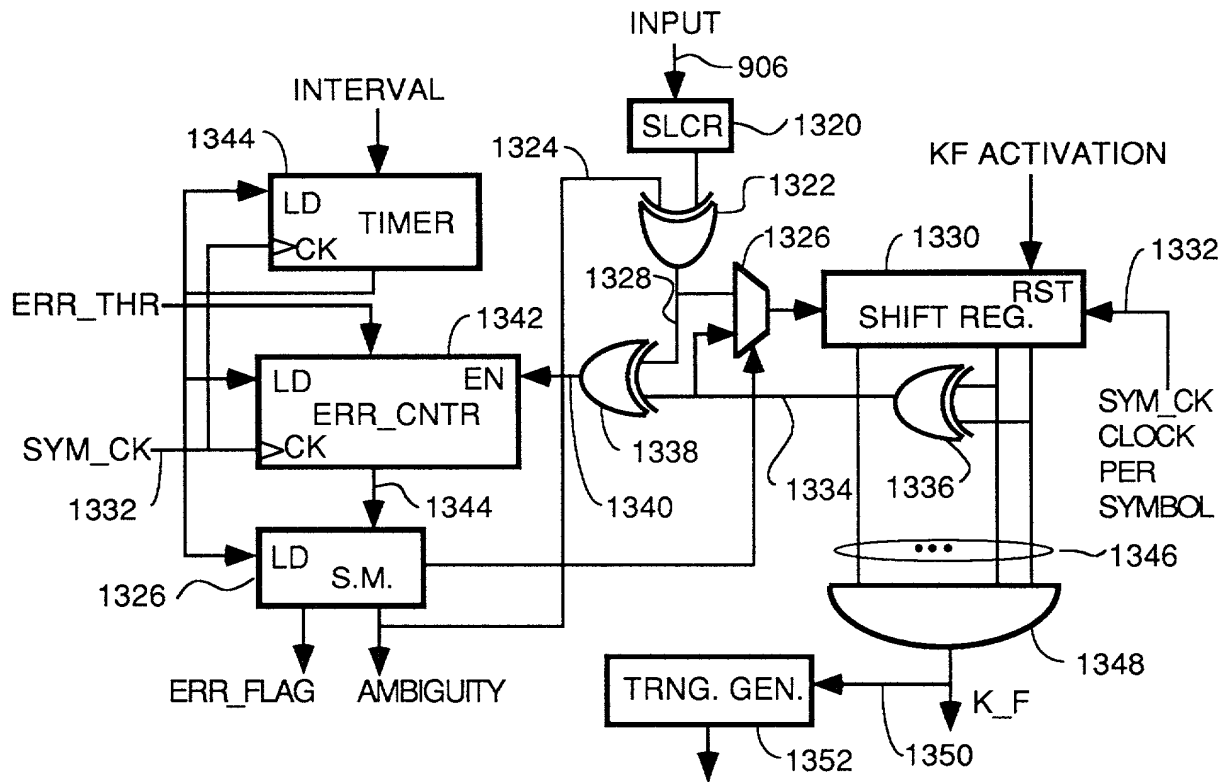
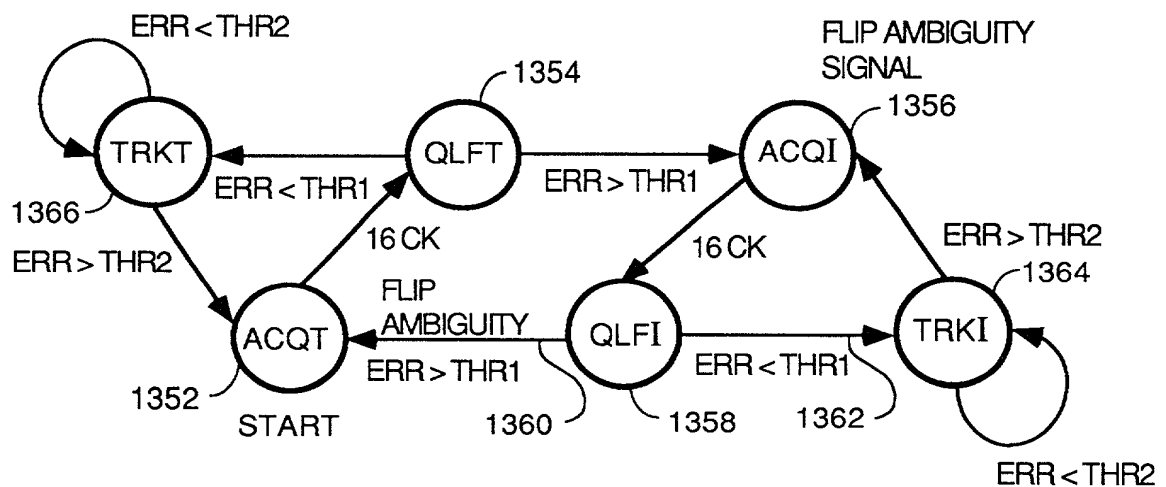


FIG. 50



FRAME DETECTOR  
FRAME SYNC/KILOFRAME DETECT

FIG. 51



STATE MACHINE

FIG. 52

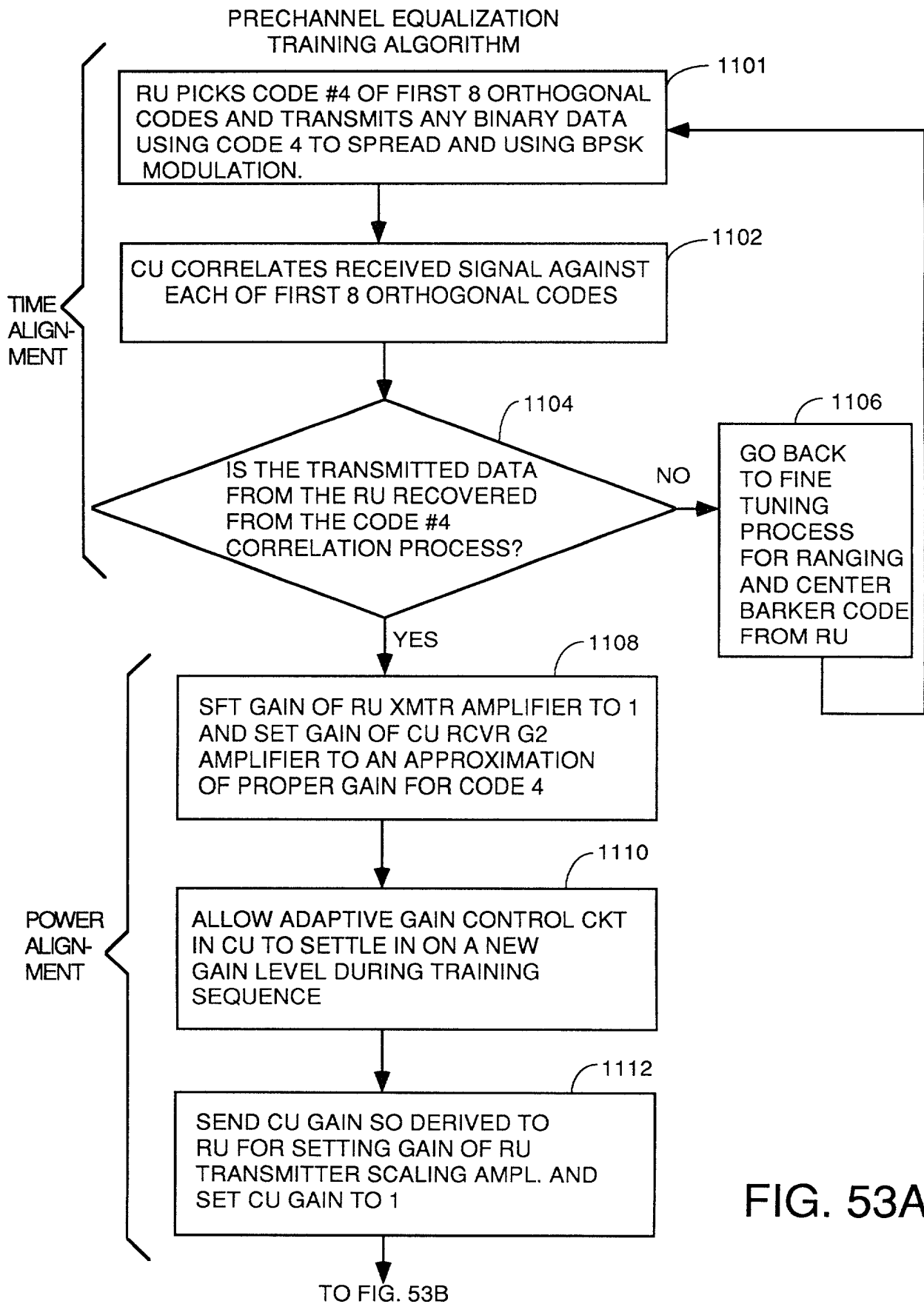


FIG. 53A



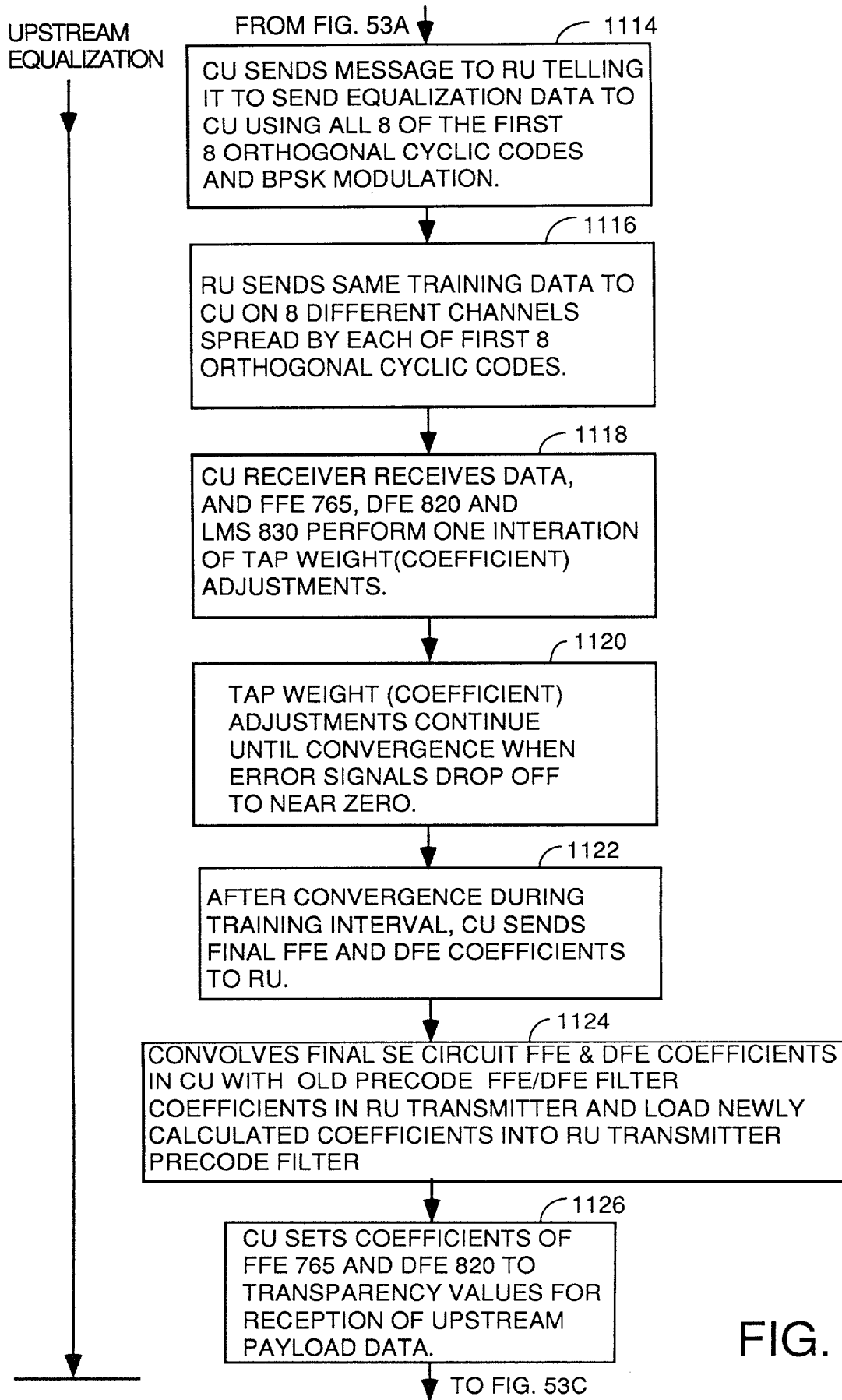


FIG. 53B

FROM FIG. 53B

DOWNSTREAM  
EQUALIZATION

CU SENDS EQUALIZATION TRAINING DATA TO RU SIMULTANEOUSLY ON 8 CHANNELS SPREAD ON EACH CHANNEL BY ONE OF THE FIRST 8 ORTHOGONAL CYCLIC CODES MODULATED BY BPSK.

RU RECEIVER RECEIVES EQUALIZATION TRAINING DATA IN MULTIPLE ITERATIONS AND USES LMS 830, FFE 765, DFE 820 AND DIFFERENCE CALCULATION CIRCUIT 832 TO CONVERGE ON PROPER FFE AND DFE TAP WEIGHT COEFFICIENTS.

AFTER CONVERGENCE, CPU READS FINAL TAP WEIGHT COEFFICIENTS FOR FFE 765 AND DFE 820 AND CONVOLVES THESE SE FILTER TAP WEIGHTS WITH THE OLD FILTER TAP WEIGHTS OF THE FFE AND DFE FILTERS OF CE CIRCUIT 764 AND LOADS THE NEWLY CALCULATED TAP WEIGHTS INTO THE FFE AND DFE FILTERS OF THE CE CIRCUIT; CPU SETS FFE 765 AND DFE 820 COEFFICIENTS TO INITIALIZATION VALUES.

FIG. 53C

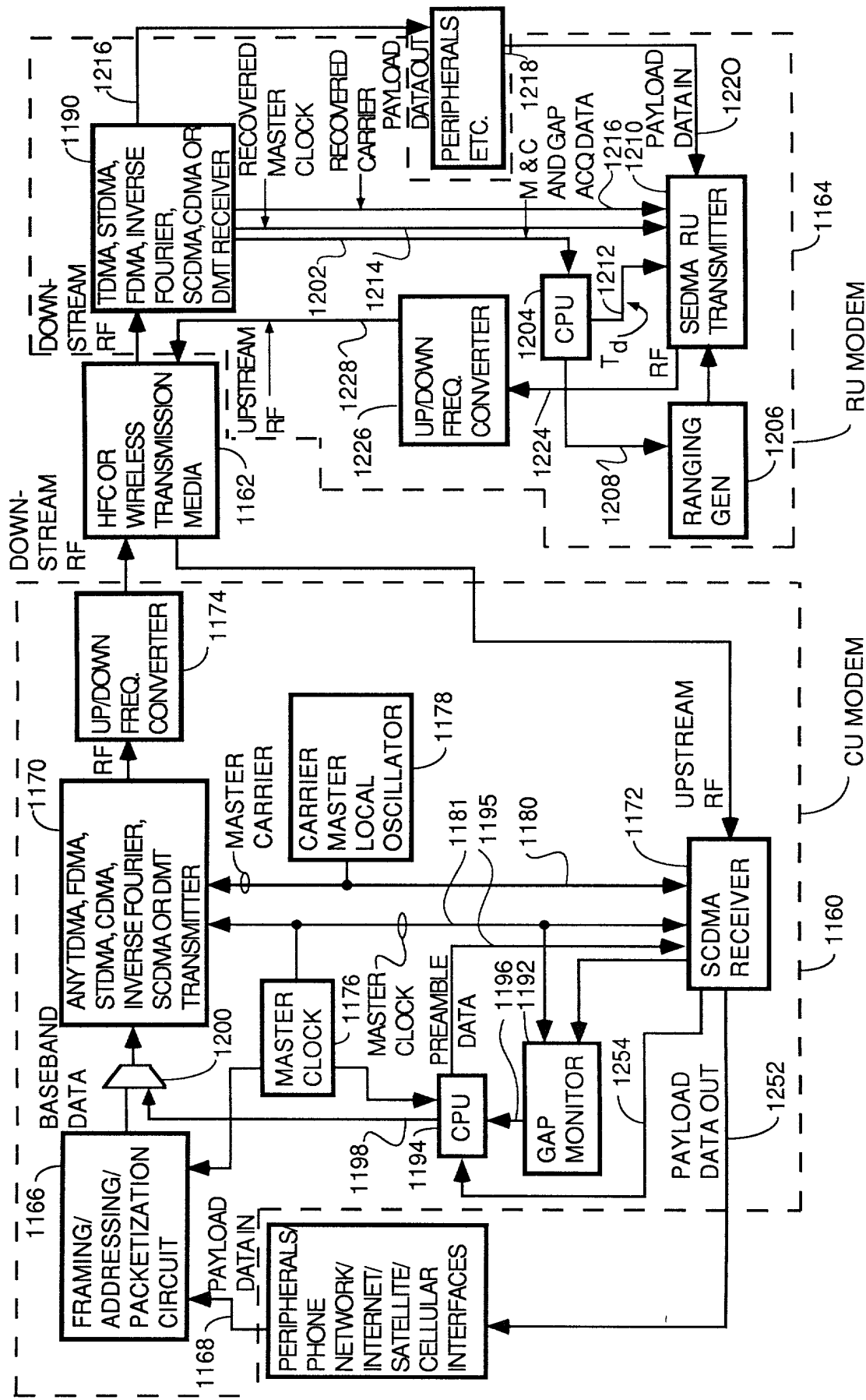
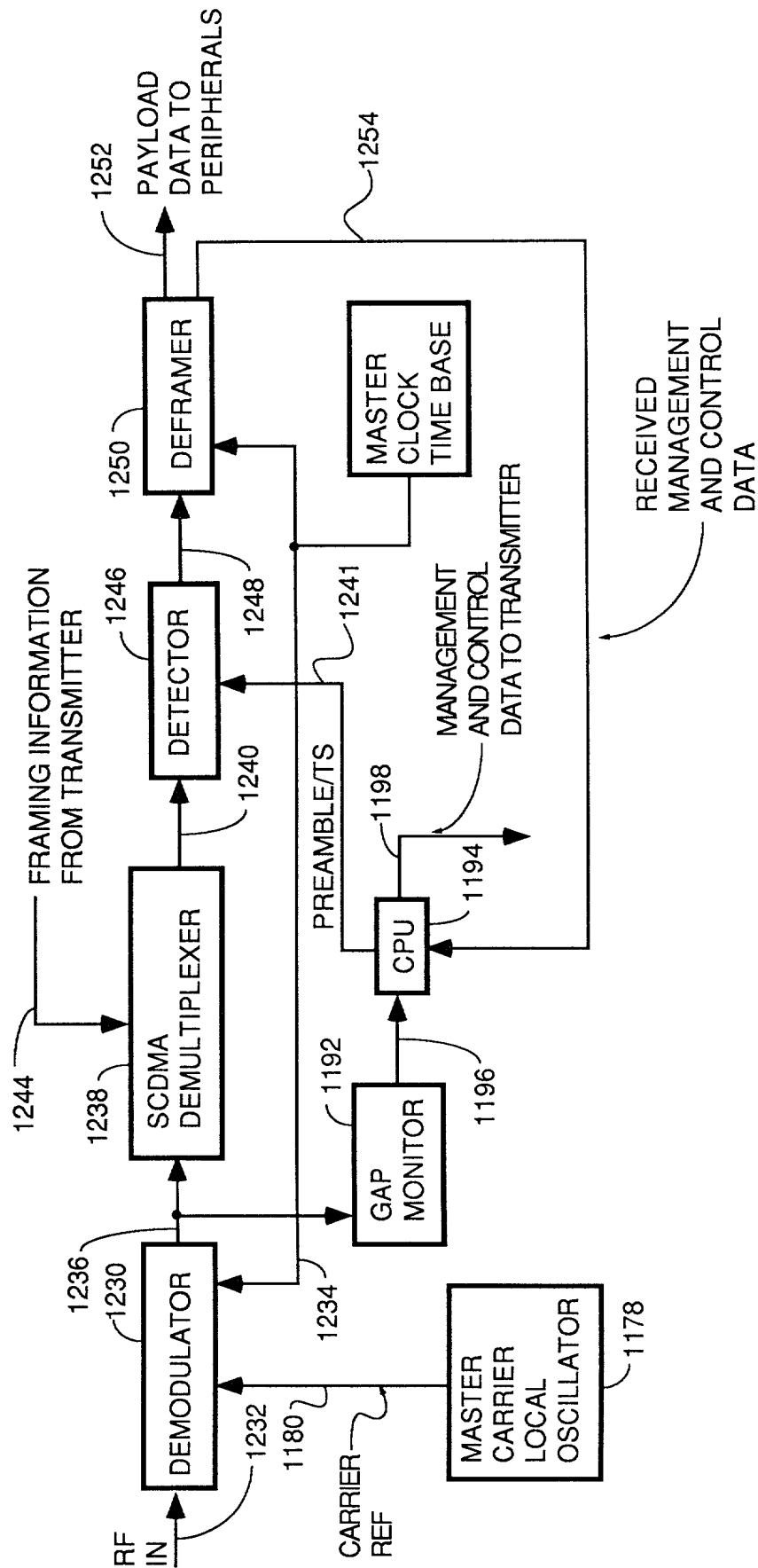


FIG. 54



SIMPLE CU SPREAD SPECTRUM RECEIVER

FIG. 55

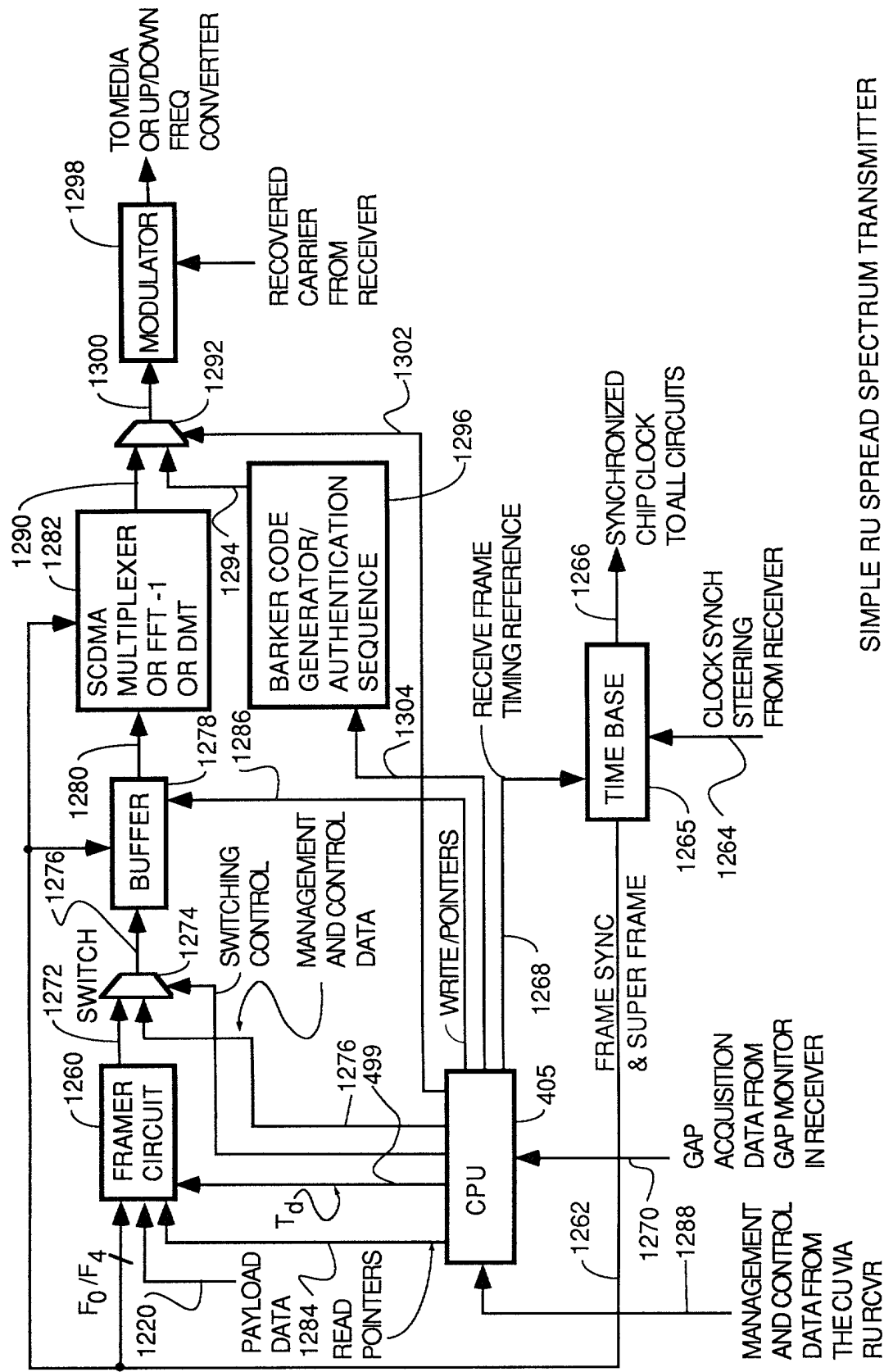
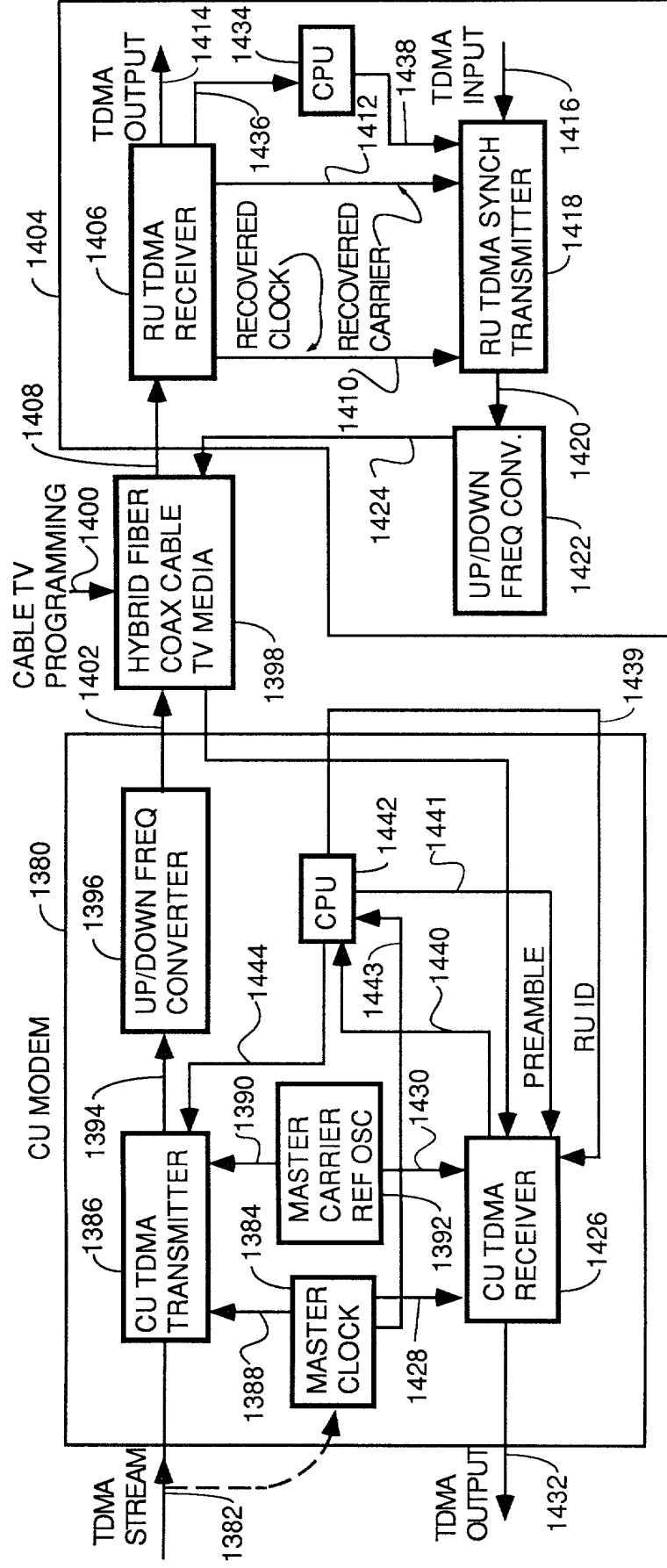


FIG. 56

SIMPLE RU SPREAD SPECTRUM TRANSMITTER



SYNCHRONOUS TDMA SYSTEM

FIG. 57

OFFSET (CHIPS)	1B ASIC		2A ASIC	
	RGSRH	RGSRL	RGSRH	RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

TRAINING ALGORITHM

SE FUNCTION

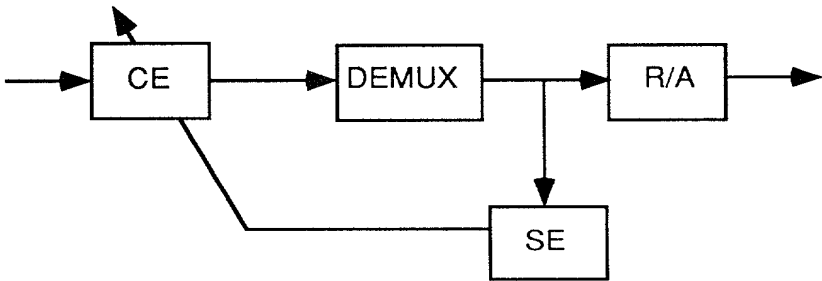
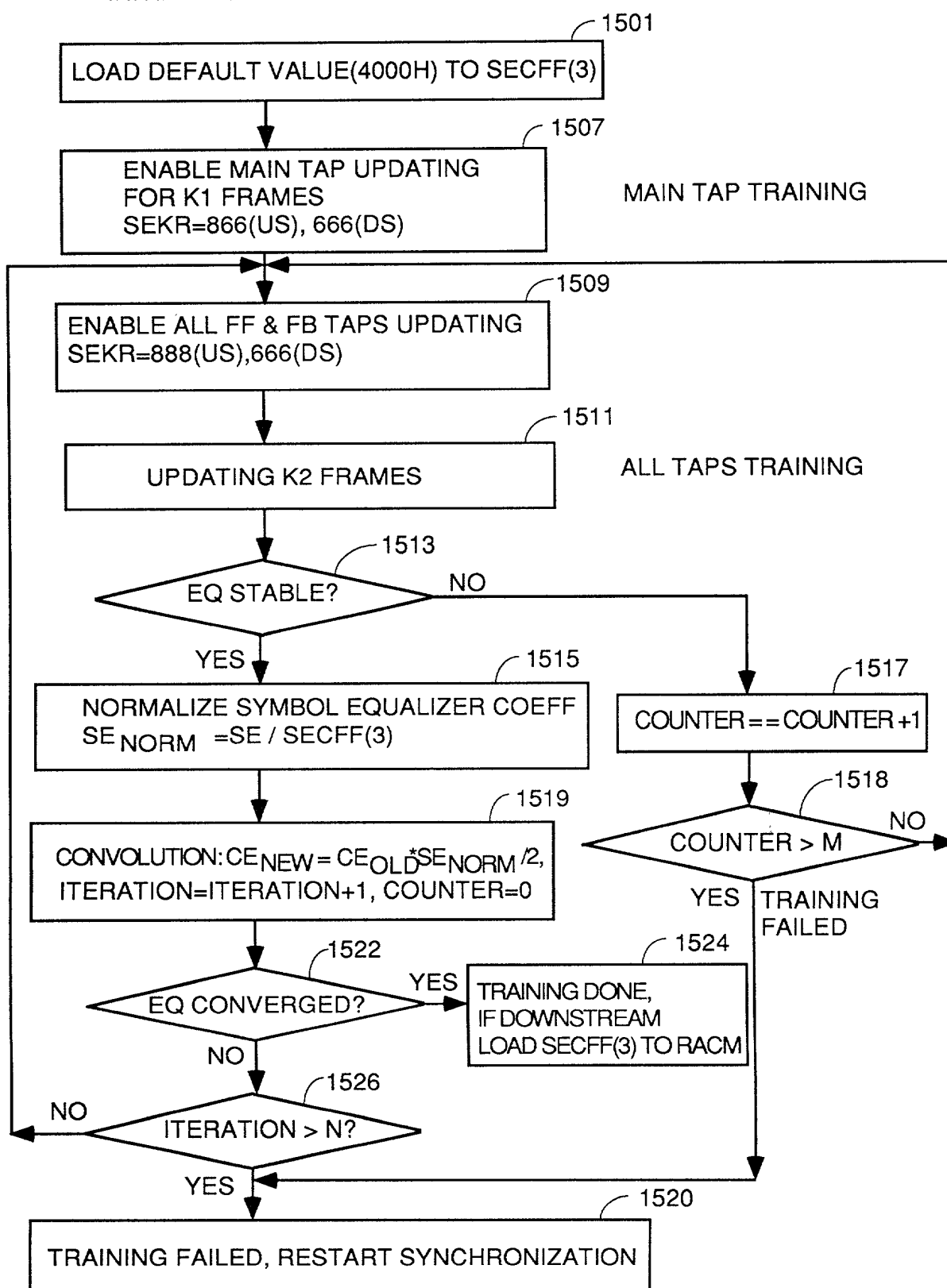


FIG. 59

# INITIAL 2-STEP TRAINING ALGORITHM



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60



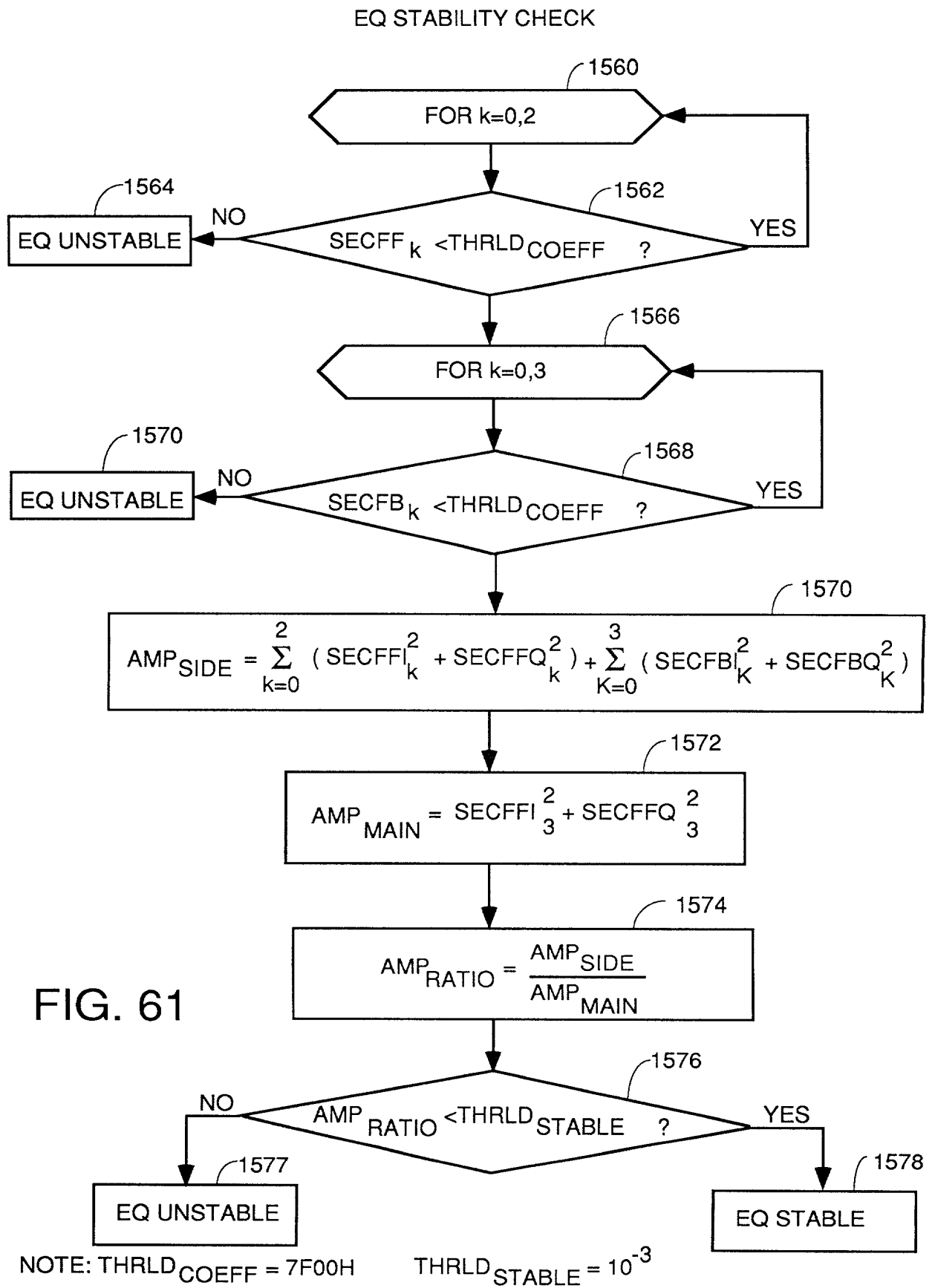


FIG. 61

# PERIODIC 2-STEP TRAINING ALGORITHM

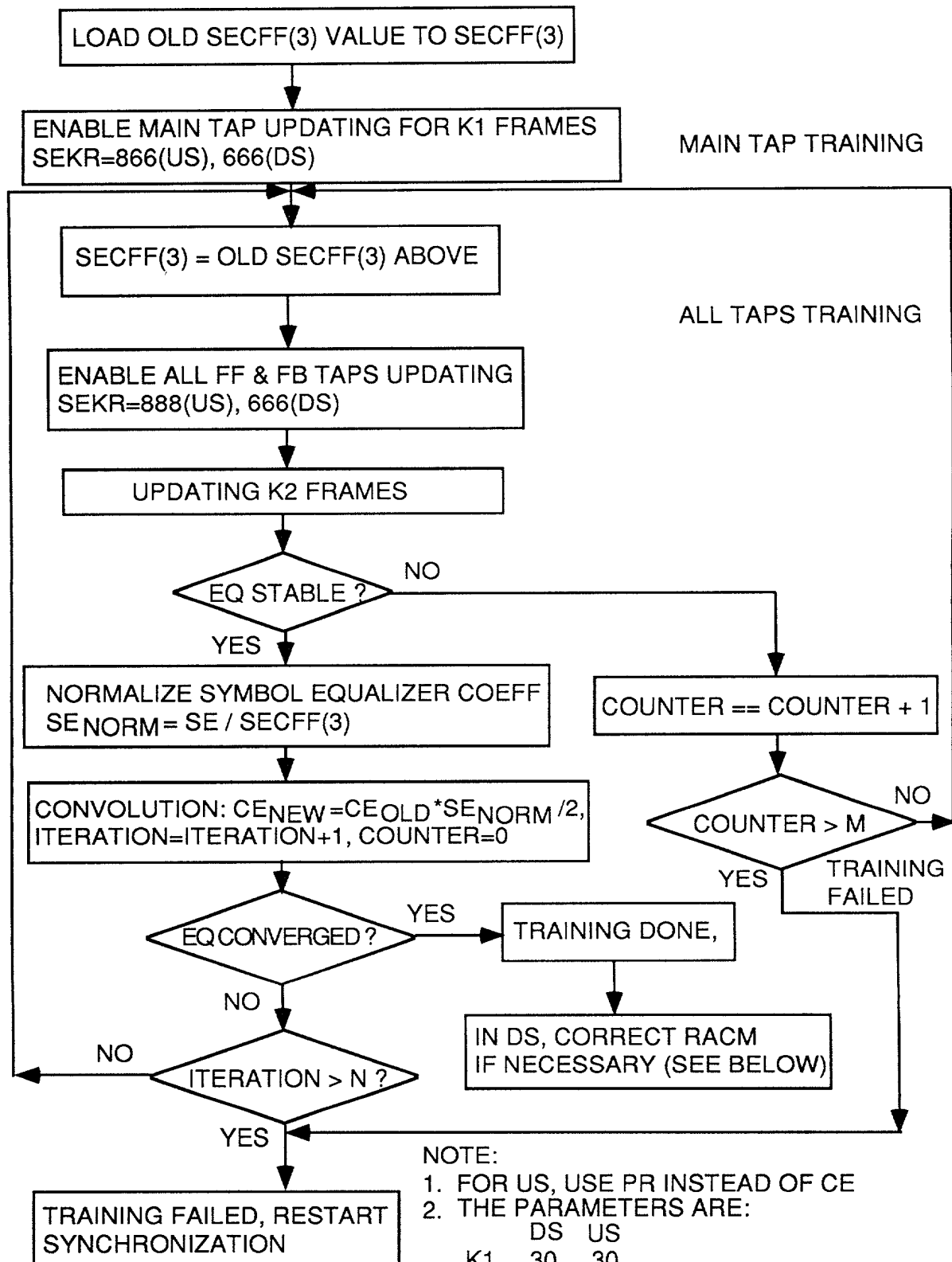
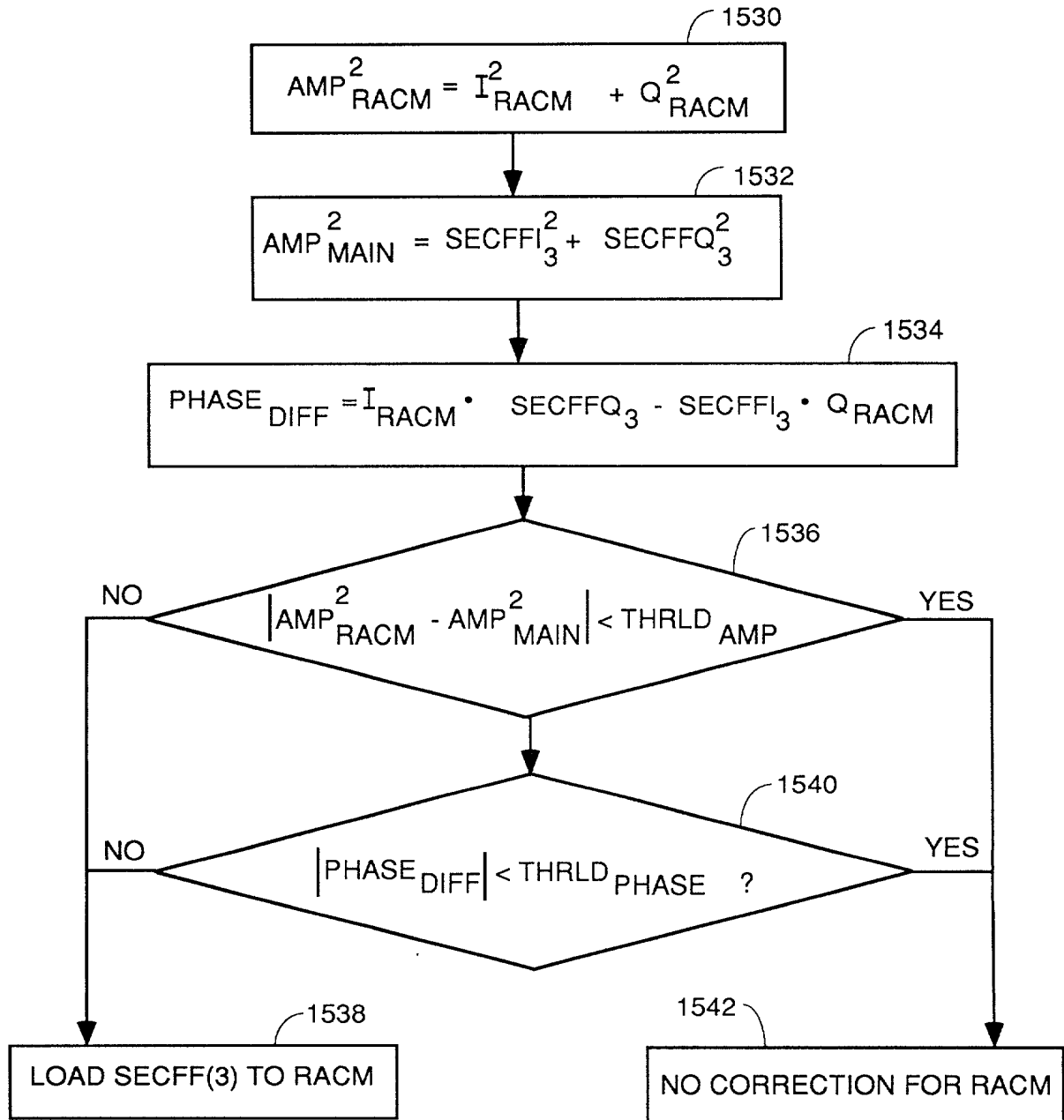


FIG. 62

09759774-041304

# RACM CORRECTION

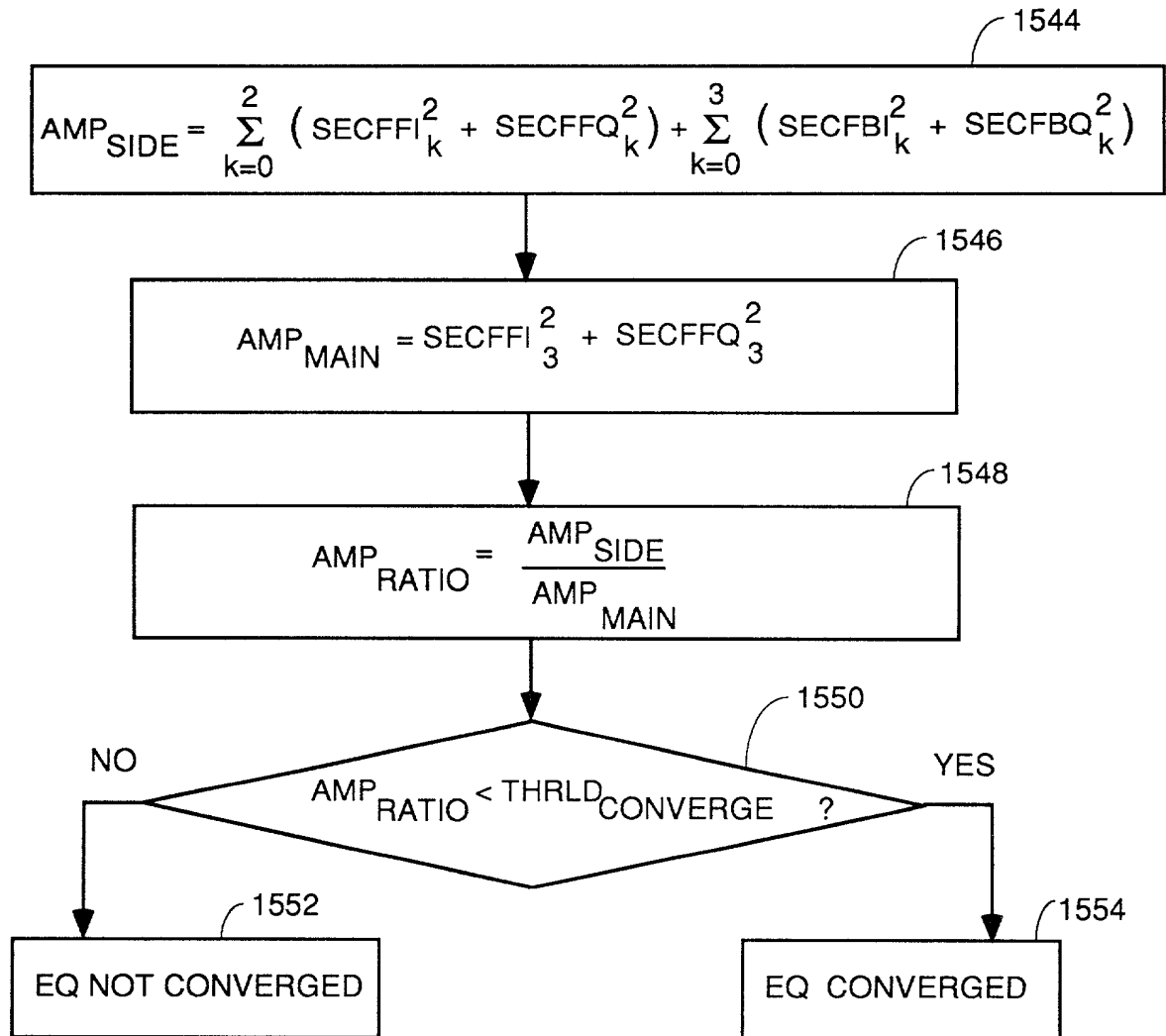


NOTE: THRLD<sub>AMP</sub> = TBD  
 THRLD<sub>PHASE</sub> = TBD

ROTATIONAL AMPLIFIER CORRECTION

FIG. 63

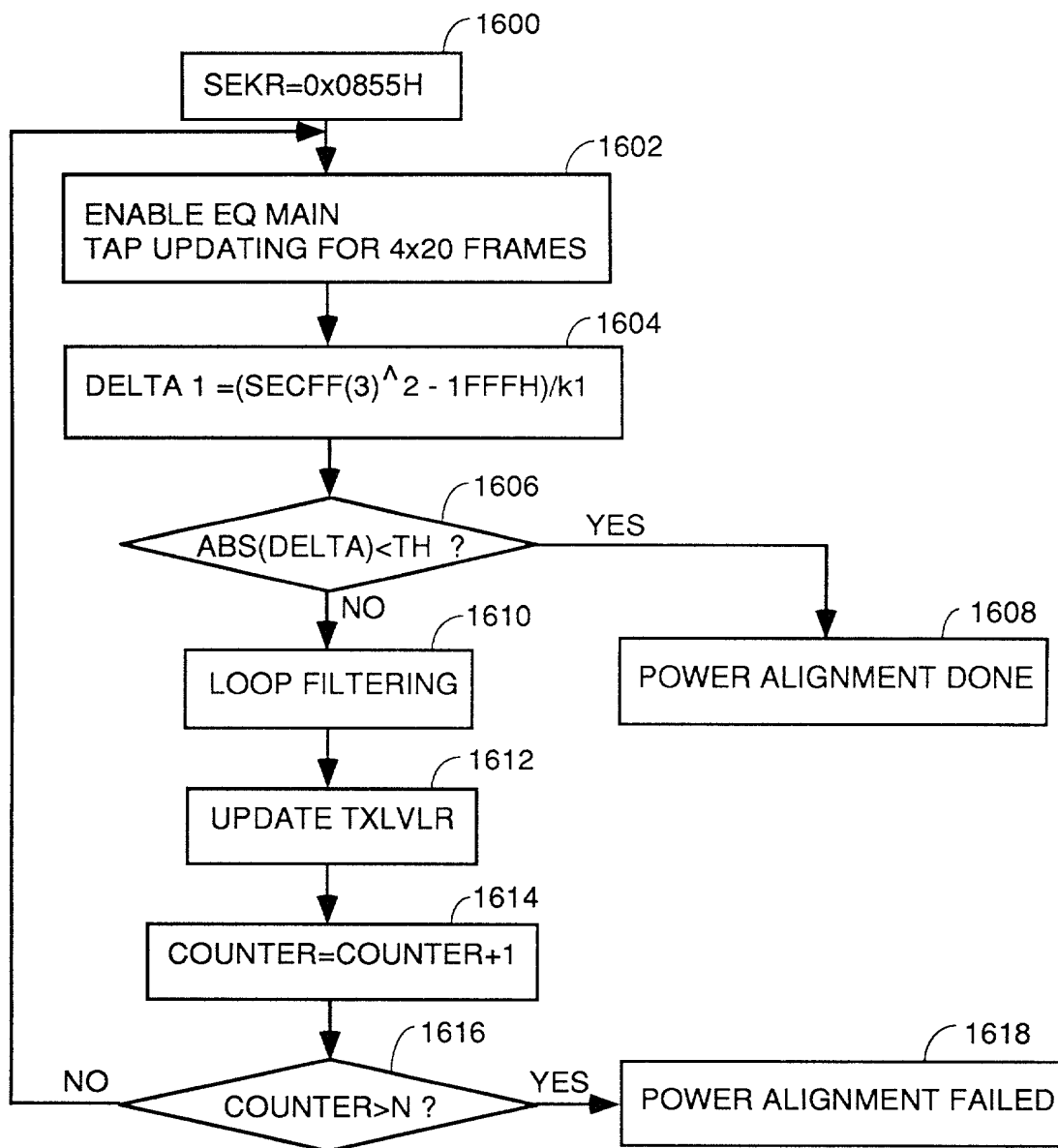
# EQ CONVERGENCE CHECK



NOTE:  $\text{THRLD}_{\text{CONVERGE}} = 10^{-5}$

FIG. 64

# POWER ALIGNMENT FLOW CHART



NOTE: TH = 600H

N = 12

FIG. 65

The diagram illustrates a network architecture for a head-end node. A central node, labeled 'CU' (1628), is connected to two other nodes: 'RU' (1624) and 'O.N.' (1620). The 'RU' (1624) is labeled '(AT HEAD-END)'. The 'O.N.' (1620) is connected to a 'FIBER' network, which in turn connects to another 'O.N.' (1622). This second 'O.N.' (1622) is connected to a 'COAX' network, which then connects to an 'RU' (1626). The 'FIBER' network is represented by a line with two upward-pointing arrows. The 'COAX' network is represented by a line with a diagonal slash. The 'RU' (1626) is connected to the 'COAX' network via a line with a diagonal slash. The 'CU' (1628) is connected to the 'O.N.' (1620) via a line with two upward-pointing arrows.

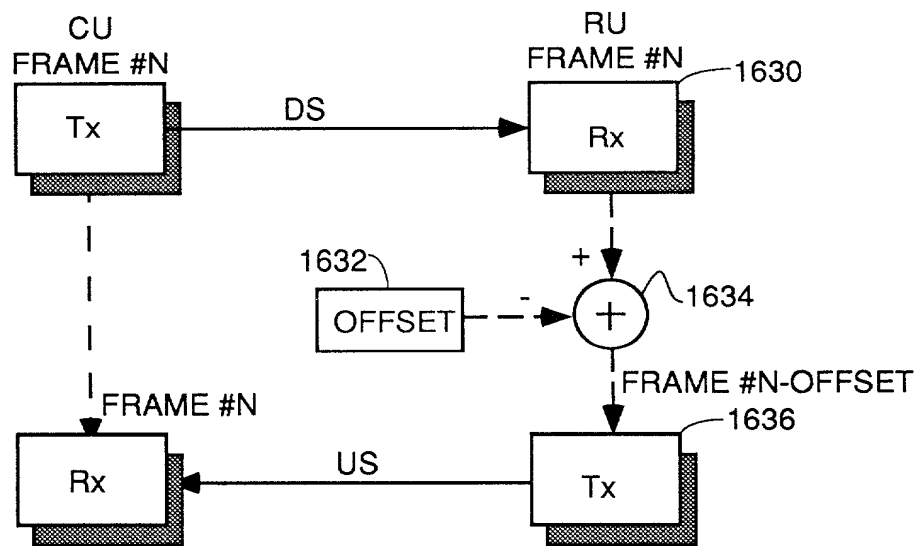


FIG. 67

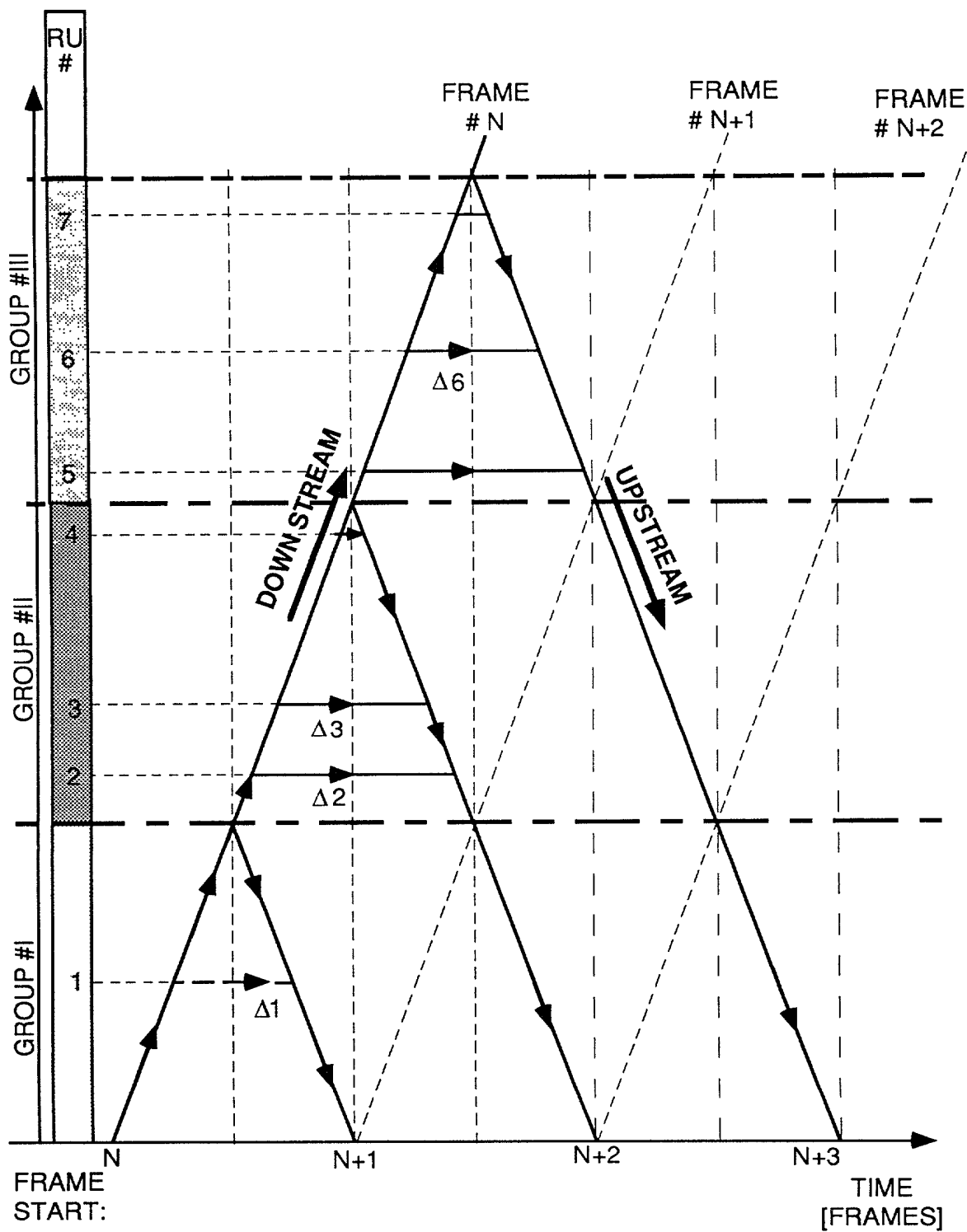
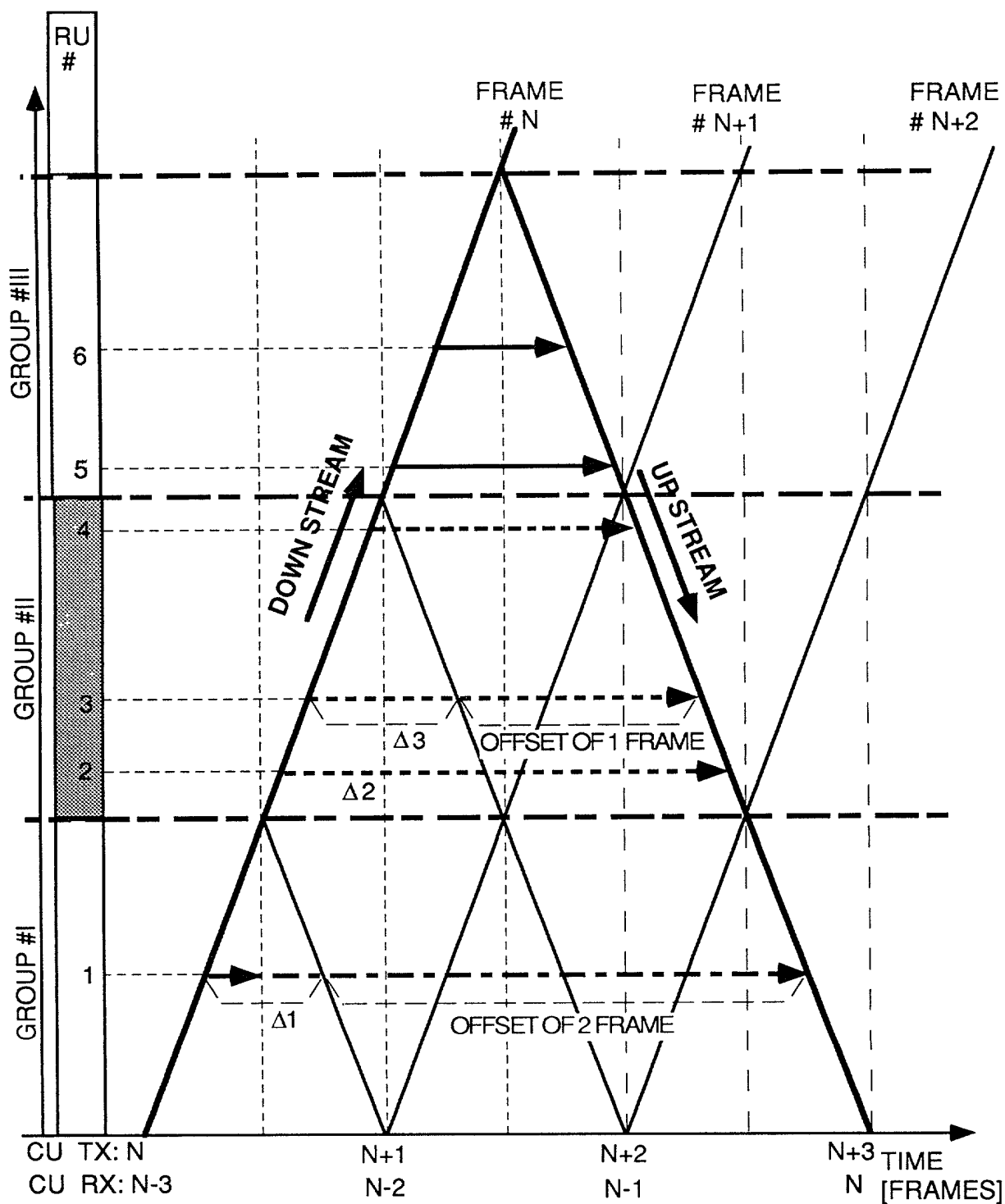


FIG. 68

FIG. 69



CONTROL MESSAGE (DOWNSTREAM) AND FUNCTION (UPSTREAM)  
PROPAGATION IN A 3 FRAMES TTA CHANNEL

FIG. 69



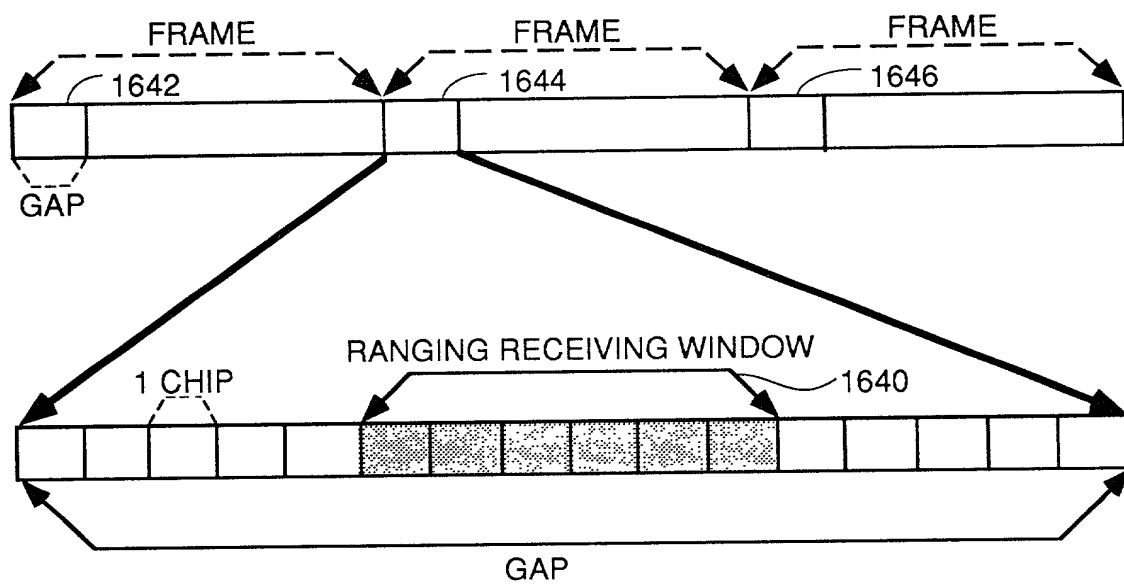
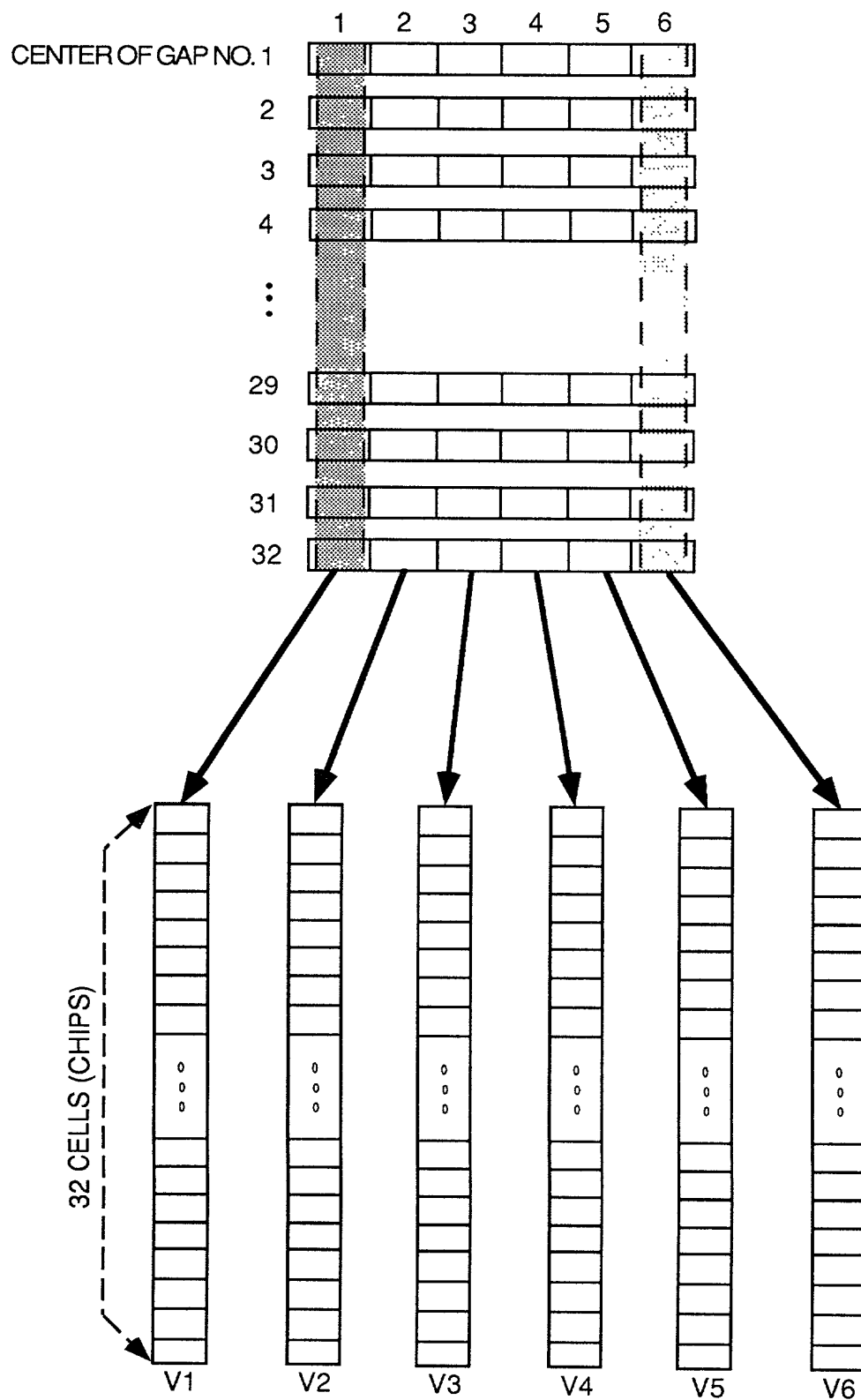


FIG. 70



OVERALL VIEW OF THE CU SENSING WINDOWS  
IN A "BOUNDLESS RANGING" ALGORITHM

FIG. 71

CHIP\FR	1	2	3	4	5	6	7		33
1	0	0	1	0	0	1	1	...	0
2	1	0	0	1	1	1	1	...	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	...	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	1	0	0	...	

FIG. 72